CPC314

CPU Module

User Manual

Rev. 001

November 2021

The product described in this manual is compliant with all related CE standards.

Product Title: CPC314
Document name: CPC314 User Manual
User Manual version: 001
Ref. docs:

Revision Record

Rev. Index	Brief Description	Product Index	Date
001	Preliminary version	CPC314	November, 2021

Contact Information

	Fastwel Co. Ltd		**Fastwel Corporation US**
Address:	108 Profsoyuznaya St., Moscow 117437, Russian Federation		6108 Avenida Encinas, Suite B, Carlsbad, CA92011, USA
Tel.:	+7 (495) 232-1681	Tel.:	**+1 (858) 488-3663**
Fax:	+7 (495) 232-1654		
E-mail:	info@fastwel.com	E-mail:	info@fastwel.com
Web:	http://www.fastwel.com/		

Table of Contents

List of Tables

List of Figures

This User Manual is designed for providing you with the operating principle and general information required for commissioning, intended use and maintenance of the CPC314 CPU Module IMES.467444.148 (hereinafter referred to as the “device” or the “product”) manufactured by Fastwel Group.

The device is made in PC/104-plus format and is designed for use in various embedded systems that require operation in an extended temperature range (from -40 to +85 °C), compatibility of applications with x86 architecture of CPUs, as well as a combination of high performance and low level of generated thermal power and power consumption.

The document is designed for developers of distributed control and data collection systems, process control systems and embedded control systems, for system administrators and engineers involved in the industrial automation area.

Ownership rights

Safety requirements

This Fastwel Group’s product is developed and tested for the purpose of ensuring compliance to the electric safety requirements. Its design provides long-term trouble-free operation. The service life of the product can be significantly reduced due to the improper handling during unpacking and installation. Therefore, in the interests of your safety and in order to ensure proper operation of the product, you should follow the recommendations below.

Conventions

Caution, High Voltage!

This sign and text warn of the dangers associated with electrical discharges (> 60 V) when touching the device or any part of it. Failure to follow the precautions mentioned or prescribed in the regulations may endanger your life or health, and may result in damages to the equipment. Please also read the below subparagraph dedicated to the rules for working with high voltage.

Attention! Static-sensitive device!

This sign and text indicate that electronic boards and their components are sensitive to static electricity, so care should be taken when handling this device and performing inspections to ensure integrity and functionality of the device.

Attention!

This sign is aimed at drawing your attention to aspects of this User Manual that, if not fully understood or ignored, may endanger your health or cause damages to the equipment.

Note

This sign is used to text fragments that should be read carefully.

Safety requirements

This Fastwel Group product has been developed and tested to ensure compliance with electrical safety requirements. Its design provides long-term fail-safe operation. The product's life cycle may be significantly shortened due to mishandling during unpacking and installation. Therefore, for your own safety and for ensuring proper operation of the device, you should follow the recommendations given below.

Rules for safe handling with high voltage

Attention!

All operations with this device should only be performed by personnel with sufficient qualifications.

Caution, High Voltage!

Before installing the board in the system, make sure that the mains power supply is off. The same also applies to the installation of expansion boards.

There is a serious risk of electric shock during installation, repairs, and maintenance of the device, so always unplug the power supply cord while carrying out of works. The same also applies to the other power supply cables.

Instructions for board handling

Static-sensitive device!

Electronic boards and their components are sensitive to static electricity. Therefore, special attention should be given when handling these devices to ensure their safety and operability.

- ✓ Do not leave the board in the non-operating position without protective packaging.
- ✓ If possible, always work with the board in workplaces protected against static electricity.

Should this not be possible, the user should remove the static charge before touching the product with their hands or tools. The best way to do so is by touching any metal part of the system enclosure.

General rules of usage

✓ In order to keep the warranty, the product must not be altered or changed in any way. Any changes and improvements unauthorized by Fastwel Group other than those contained in this User Manual or received from the technical support service of Fastwel Group in the form of a set of instructions for their implementation will void the warranty.

✓ This device should be installed and connected only to systems that meet all necessary technical and climatic requirements. This also applies to the operating temperature range of a particular version of the board. You should also consider the temperature limits of the batteries installed on the board.

✓ Follow the instructions in this User Manual only when performing all necessary installation and configuration operations.

✓ Retain the original packaging for storing products in the future or to transport in case of a warranty claim. If it is necessary to transport or store the board, pack it the same way as it was packed at the time of receipt.

✓ Proceed with extra caution when handling and unpacking the device. Follow the instructions given below.

✓ It is not allowed to connect external equipment, communication interface cables without disconnecting the power supply of the product and connected external equipment.

MANUFACTURER'S WARRANTIES

Warranty liabilities

The manufacturer guarantees that CPC314 meets the requirements of technical specifications of the "CPU MODULE IN PC104 FORMAT" TU 4013-004-52415667-05 provided that the Consumer complies with the operating conditions, transportation, storage, installation and mounting, set by the operational documents.
The manufacturer guarantees that the products supplied by it will not show any manufacturing defects and materials used in compliance with the rules of operation and maintenance during the warranty period established at the moment. The Manufacturer's obligation under this warranty is to repair or replace, free of charge, any defective electronic component included in the returned product.
Products that failed through the Manufacturer's fault during the warranty period will be repaired free of charge. In other cases, the Consumer will be billed based on current remuneration rates and the cost of consumables.

Right of limitation liability

The manufacturer is not responsible for any damages caused to the Consumer's property due to the failure of the product in the process of its use.

Warranty period

The warranty period for the manufacturer's products is 36 months from the date of sale (unless otherwise provided by the delivery agreement).

For customized products, the warranty period is 60 months from the date of sale (unless otherwise provided by the delivery agreement).

The warranty set forth above does not extend to and shall not apply to:

1. Products, including software, which have been repaired or altered by other than Fastwel personnel, unless Buyer has properly altered or repaired the products in accordance with procedures previously approved in writing by Fastwel.
2. Products, which have been subject to power, supply reversal, misuse, neglect, accident, or improper installation.

Returning a product for repair

1. Apply to Fastwel Company or to any of the Fastwel's official representatives for the Product Return Authorization.
2. Attach a failure inspection report with a product to be returned in the form, accepted by customer, with a description of the failure circumstances and symptoms.
3. Carefully package the product in the antistatic bag, in which the product had been supplied. Failure to package in antistatic material will VOID all warranties. Then package the product in a safe container for shipping.
4. The customer pays for shipping the product to Fastwel or to an official Fastwel representative or dealer.

Transportation, Unpacking and Storage

Transportation

The modules should be transported in the separate manufacturer's packaging (container), consisting of an individual antistatic packaging and a cardboard box, in closed transport (road, rail, air in heated and sealed compartments) under storage conditions 5 according to the GOST standard 15150-69 or under storage conditions 3 for sea transportation.

It is allowed to transport the modules packed in individual antistatic bags in manufacturer's group packaging (container).

Transportation of packaged modules should be carried out in accordance with the rules of transportation of goods currently valid for this type of transport.

During handling operations and transportation, the packed modules should not be subjected to sudden shocks, drops, impacts and precipitation. The packed modules should be placed on the vehicle in such a way as to preclude their further movements.

Unpacking

Before unpacking, after transportation at negative ambient temperatures, the modules must be kept for 6 hours under storage conditions 1, in accordance with the GOST standard 15150-69.

Do not place the packed modules near any heat sources before unpacking.

When unpacking the modules, it is necessary to observe all precautions to ensure their safety, as well as marketable condition of manufacturer's consumer packaging.

When unpacking, it is necessary to check the modules for any external mechanical damages after transportation.

Storage

Storage conditions of the modules 1 comply with the GOST standard 15150-69.

1 Description and operation

1.1 Purpose of the device

The device is a highly integrated solution based on the x86 platform for the use in real time systems of management, production control, data acquisition and processing and can operate in the standalone and slave mode. Connection of the main I/O means (VGA monitor, LVDS panel, keyboard, mouse, printers, USB) enables the device to be used in systems with operator participation. For data storage, both a microSD card integrated into a socket and an external storage device connected to SATA port, or external USB devices can be used.

The product is made in PC/104-*plus* format and enables you to solve most of the tasks of input-output of digital signals and information processing. Expanding device's functionality is also possible by connecting additional expansion modules of the PC/104 and PC/104-*plus* format.

The product can be connected to RS-232, RS-485 and Ethernet networks, which makes it possible to use it in distributed input-output and information processing systems.

1.2 Technical specifications

- **Vortex86DX3 CPU (x86-compatible instruction set):**

- Clock rate: 800 MHz;
- Number of physical cores: 2;
- 32 x bit x86 core;
- 32 bit memory bus;
- L1 cache (64 KB);
- L2 cache (512 KB);
- Internal bus frequency: 100 MHz

- **RAM:**

- DDR3 SDRAM 2 GB (soldered onboard);
- Memory bus width: 32 bit;
- Memory bus operating frequency: 667 MHz;

- **Video subsystem:**

- video controller with 2D accelerator;
- port for connection of VGA monitor with resolution up to 1920x1440, color 32 bit;
- port for connection of LVDS panel with resolution up to 1920x1440, color 32 bit;

- **Audio port:**

- port for mic connection (mono);
- Line-in, Line-out ports (stereo);

- **PCI104 bus:** (PCI 33 MHz 32 bit);
- **PC104 bus:** (ISA 8/16 bit, 8/16 MHz);

- **Non-volatile RAM:**

- volume: 8 KB;
- implemented using the FRAM technology, SPI interface;
- battery power supply is not required;

- **Connector for microSD cards:**

- support of SD, SDHC cards, speed class 6;
- microSD 4 GB (pSLC NAND), already installed when delivered;
- the card is defined as Primary IDE Master within the system;

- **Port for SATA drive:**

- standard SATA connector;
- 1.5 Gb Gen I and 3 Gb Gen II;

- **LAN ports:**

- 2 x Fast Ethernet 10/100 Mb/s ports;
- system isolation of each port: 500V;

- **USB ports (host):**

- support of USB 1.1, USB 2.0 (HS, FS, LS);
- connection of up to 2 devices;

- **GPIO port**

- 8 x I/O lines;
- compatibility with the level +5V (TTL);

- **LPT port**

- **Serial ports:**

- **COM1**: RS-232 (9-wire);
- **COM2**: RS-232 (9-wire);
- exchange rate over RS-232: up to 230,400 Kb/s;
- protection against ESD 15 kV (IEC1000-4-2);
- **COM3**: isolated RS-422/485 (individual system isolation 500V);
- **COM4**: isolated RS-422/485 (individual system isolation 500V);
- automatic (hardware) control of transmission direction for RS-485 ports;
- exchange rate over RS-422/485: up to 1.5 Mb/s [1]

- **Watchdog timers:**

- 2 watchdog timers, built into the processor, with a programmable event and an actuation interval of 30.5 μs…512 s;

- **Real Time Clock:**

- consumption current when power is off 2 μA[2]

- **Integrated lithium battery 3V:**

- CR2032, standard capacity 200 mA*h;

- **Buzzer**

- **Isolated port of reset / interrupt source**

[1]Exchange rate over serial ports is defined by the frequency divider register.
[2] Standard value under normal conditions

- **Digital temperature sensor**

Measuring the temperature of the CPU board from - 55 to +125 °C,
Typical absolute error of temperature measurement:[3]
± 2.0 °C (within the range from -40 to +85 °C);
Conversion code – additional, with a character
Resolution and price per unit fort the least significant bit: 12 bit (11+ character) / 0.0625 °C
Conversion time is up to 300 ms.

- **Measuring secondary supply voltages of the module by an integrated ADC**
- **Compatibility with operating systems:**

- FreeDOS, Microsoft™ MS-DOS® 6.22
- Linux
- Windows Embedded Standard 7

- **Console serial ports:** COM1 / COM2 / COM3 / COM4;
- **Power supply voltage:** from 4.75 to 5.25 V
- **Operating temperature range:** from -40 to +85 °C
- **Storage conditions for the modules:** 1 according to the GOST standard 15150-69
- **Humidity:** from 5 to 95%, at +25 °C, non-condensing;
- **Resistance to multiple/single shocks:** 50/150 g;
- **Vibration resistance:** 10 g for frequencies from 50 to 2000 Hz;
- **MTBF [4]:** min. 100,000 hours;
- **Dimensions, max:** (115.6±0,5) x (102.2±0,5) x (24.2±0,5) mm;
- **Module's weight, max.:** 0.2 kg;
- **Packed weight, max.:** 0.4 kg;

1.3 Connection to the device

Below is the typical list of interface boards and devices, which may be connected to the device:

- Devices with Ethernet interface;
- Devices compatible with RS-232 and RS-422;
- RS-485 multiuser networks;
- microSD memory cards;
- SATA drives;
- USB devices, type 1.1 and 2.0 (Full-speed, High-speed), including devices of the USB Mass Storage Device type;
- Keyboard, mouse (USB and PS/2 ports);
- Monitors and TFT panels;
- PC-compatible printer (USB or LPT port);
- Expansion modules in PC/104 or PC/104-plus format.

[3] The measurement accuracy is not standardized and is determined by the data given in the manufacturer's documentation.
[4] The MTBF value is calculated using the Telcordia Issue 1 calculation model (Method I Case 3) for continuous operation when located on the ground under conditions corresponding to the climatic category Moderately Cold Climate 4 in accordance with GOST 15150-69 standard, at an ambient temperature of +30°C.

1.4 Power Supply

The device's power supply should meet the requirements specified in Table 1-1.

The device is powered through the PC/104 and PC/104-plus connectors (if installed). If you need to supply power from an external source, you can use the additional XP7 power supply connector (4-pin AMP 4-171826-4 connector).

The power supply should provide the starting current specified in Table 1-1. It is also permitted to use a power supply with a current limiting mode for at least 3.0 A (excluding any peripherals connected). When choosing a power supply, the starting current and the current consumption of expansion modules and other devices connected to the device ports, should be considered.

The device is equipped with an active circuit for protection against short circuit and reverse voltage supply. There is also a surge protection against overvoltage above 30 V (direct or reverse polarity) by parallel connection of the TVS protection diode SM6T33CA. In case of a long-term supply of more than 30V supply voltage (direct or reverse polarity), the TVS protection diode may fail. The duration of the voltage supply where the TVS protection diode fails depends on the level of the supplied voltage and the ambient temperature: at an ambient temperature of 24°C and an input voltage level of up to 60V, failure is possible in one second, at the level of up to 120V - in less than one second.
There are following consumers of the +5 V input power supply:

1) Device (+5V @ 1.5A);

2) External equipment connected to USB ports (4x ports, maximum consumption of each port is +5V @ 0.5A);

3) External equipment, connection to LPT port (1 x port, maximum consumption of each port is +5V @ 0.75A);

4) LVDS panel (1 x port, maximum consumption of +3.3V @ 0.75A);

5) External equipment, connection to GPIO port (maximum consumption of +5V @ 0.75A);

6) External equipment, connected to RS-232 ports (2 x ports, maximum consumption of +5V @ 0.75A).

The maximum possible load-carrying capacity for the "+5 V" power supply voltage is 5 A. If the 6A value is exceeded, the active protection of the device will be triggered and the input power will be disconnected, which will be automatically restored when the load current falls below the 6A limit value, in which case the device will restart.

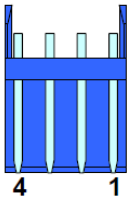
Table 1-1 - Requirements for the external power supply parameters

Version	Power supply voltage, V	Voltage limiting values, V	Load current, A	Start-up current, A
CPC314-01 without peripherals	+5V	from +4.75 to +5.25	2.0	3.0

Recommended mating part for additional XP11 power connector (AMP 4-171826-4): AMP 4-171822-4 and AMP 170263-1 sets of pins (available for order as ACS00038 kit (socket and pins) or as ACS00038-01 kit (socket , pins and 1m long wires).

Table 1-2 – Purpose of the power supply connector pins

Power supply connector: AMP 4-171826-4	
Pin#	**Function**
1	+5 V
2	GND
3	GND
4	-



1.5 Block diagram

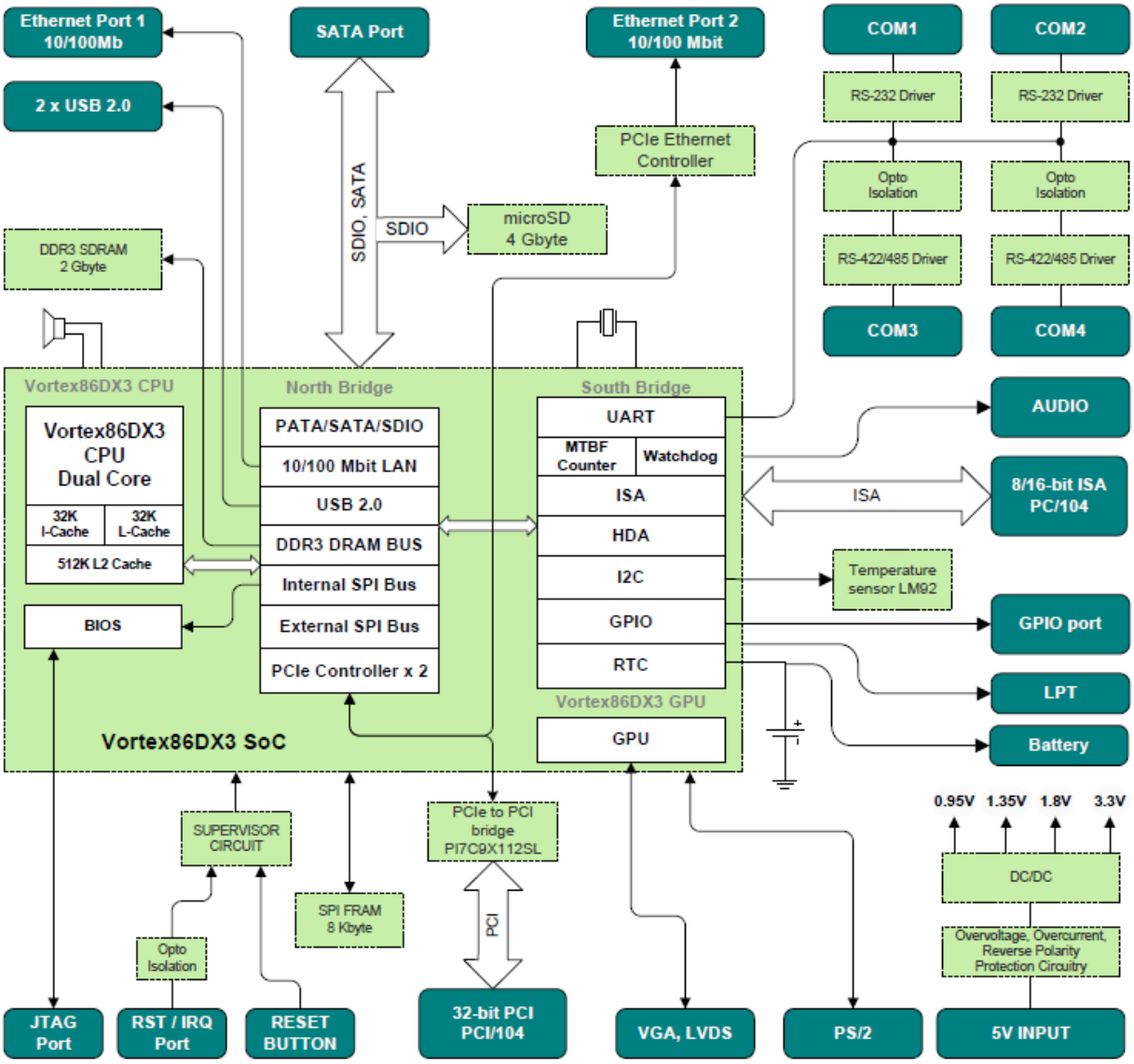


Fig. 1-1 – Block diagram of the device

1.6 Overall and fitting dimensions

Fig. 1-2 below demonstrates overall and fitting dimensions.

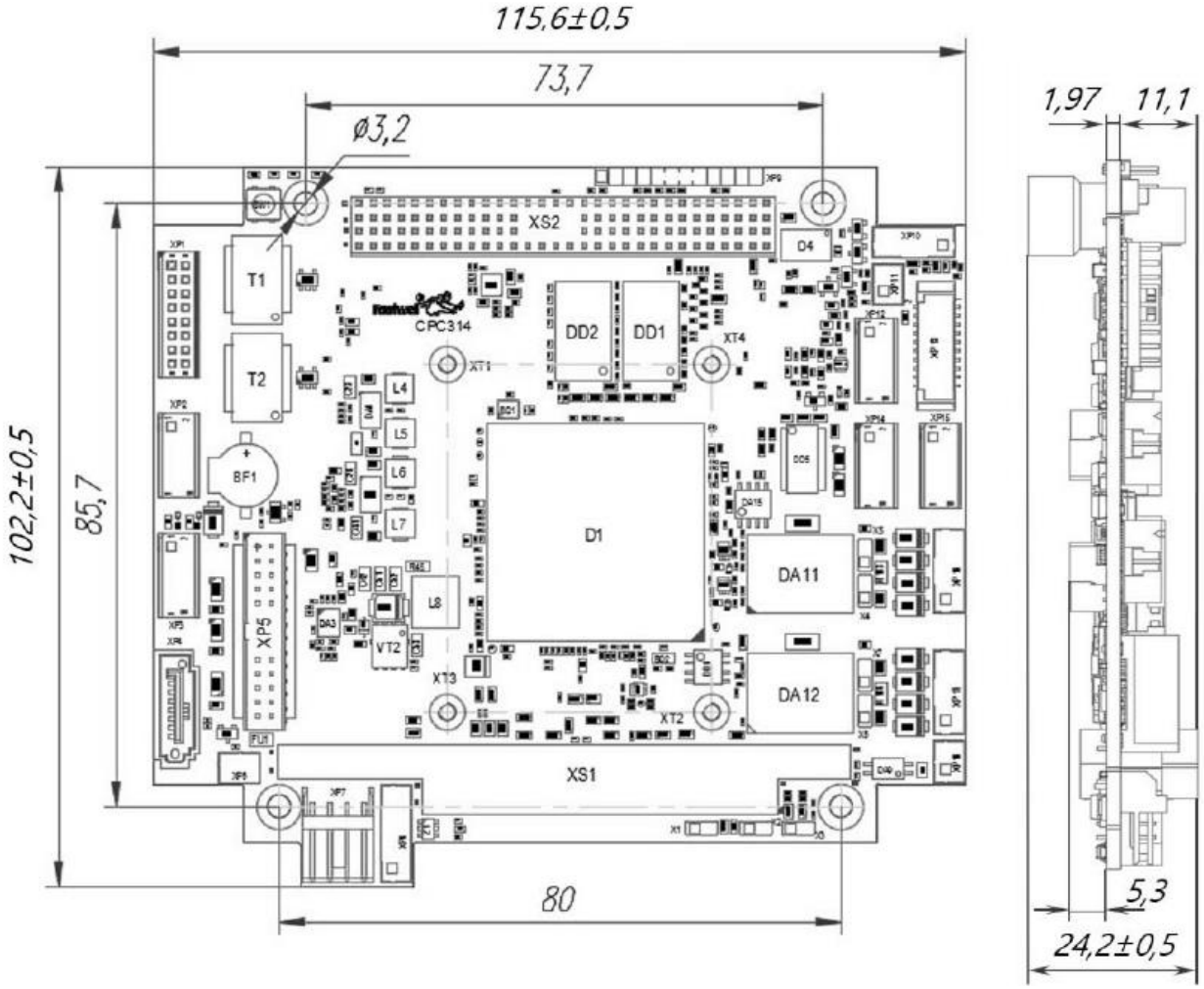


Fig. 1-2 – Overall and fitting dimensions

1.7 Location of main elements

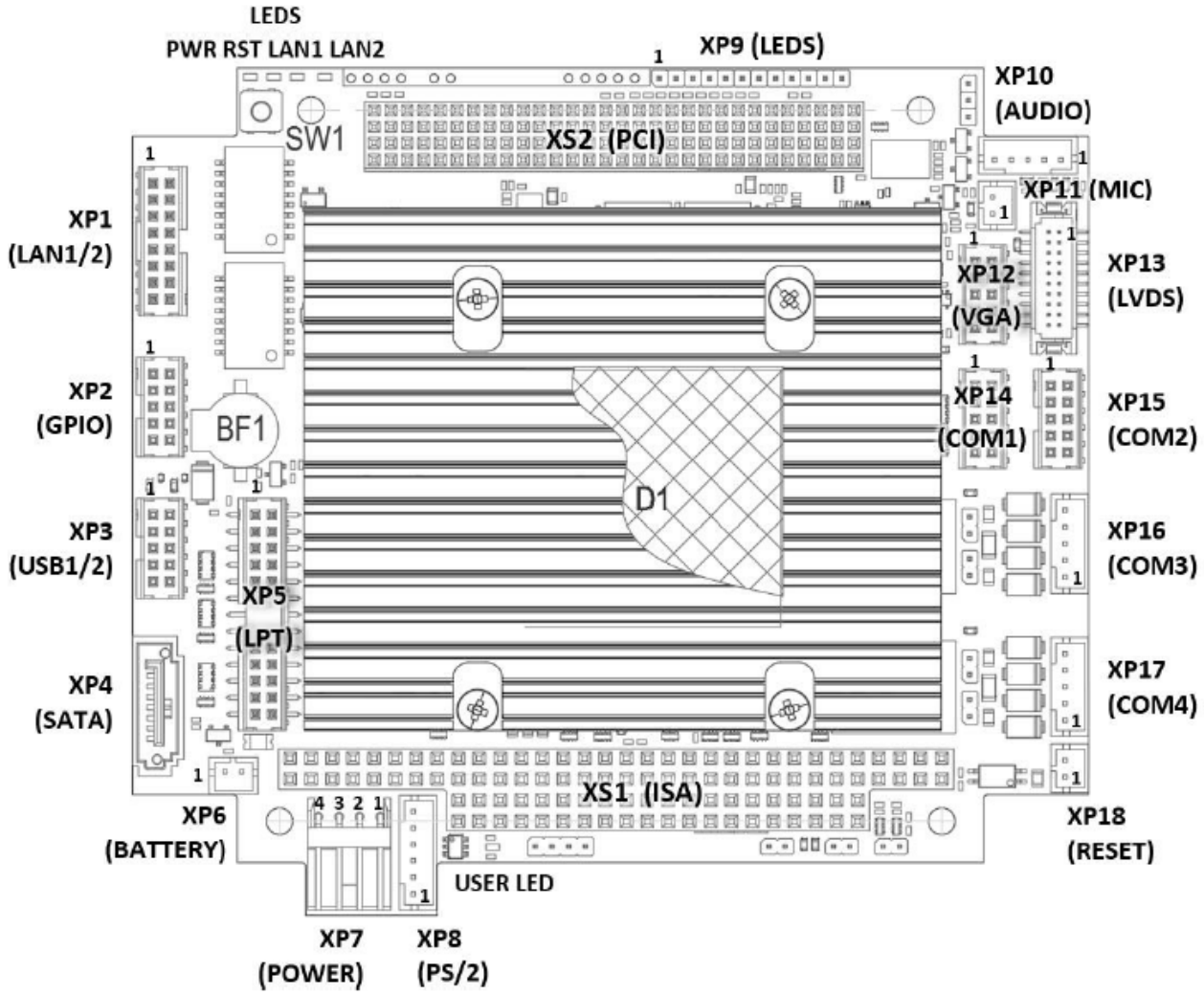


Fig. 1-3 – Location of main elements of the device on the top side of the board

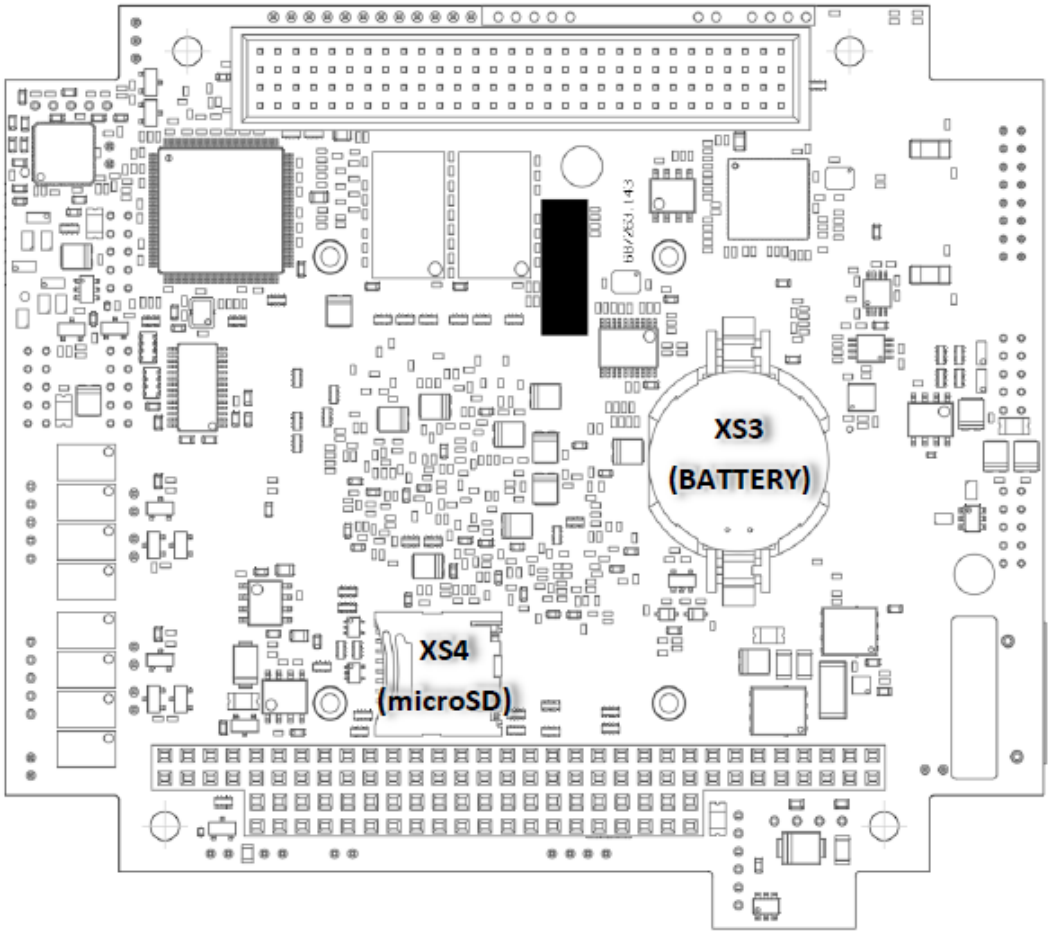


Fig. 1-4 Location of the main elements of the device on the bottom side of the board

The assignment of connectors and switches is given in **paragraph 1.10 Structure and functioning** and paragraph **3.1 Setting the switches**.
The device is made in accordance with the *PC/104-plus* v.2.0 specification.
On the top side, there is a deviation from the specification for the maximum height of components (8.76 mm) and in the area of the processor's heatsink: 10.8 mm.

On the bottom side, there is a deviation from the specification for the maximum height of the components (4.83 mm) in the area of XS3 mounting for the CR2032 battery: 5.30 mm.

1.8 Versions

Item No.	Version	Description
1	CPC314-01 IMES.467444.148	PC/104+, Vortex86DX3 800MHz, 2GB RAM, microSD 4GB, 2 x LAN, 2 x USB, VGA, PS/2, LPT, 2 x RS-232, 2 x RS-485, 8 x GPIO, FreeDOS

Note

The modules with conformal coating obtain the "\COATED" inscription when ordered.

1.9 Delivery checklist

The standard delivery checklist includes:
1. CPC 314 CPU Module
2. Installation kit – 1 pcs.
3. Packaging.

The installation kit for IMES.467941.055 includes:

1. Jumper – 10 pcs.
2. Rack WE – 4 pcs.
3. DIN7985-M3x6-A2 screw – 4 pcs.
4. DIN985-M3-A2 nut – 4 pcs.
5. DIN125-3,2-A2 washer – 4 pcs.
6. DIN6798A-3,2-A2 washer – 4 pcs.

1.10 Structure and functioning

1.10.1 Processor

The device is based on a dual-core x86-compatible 32-bit Vortex86DX3 processor with low power consumption, made using 45nm technology. The operating frequency of the processor is 800 MHz. The detailed information on the processor, as well as the current versions of drivers and system software can be found on the manufacturer's website at: http://www.vortex86.com.

1.10.2 Supervisor, Watchdog, Reset

The device includes a power supply supervisor (a microchip that monitors the power supply voltage of the device), as well as 2 watchdog timers integrated into the CPU (WDT0, WDT1). The supervisor generates a hardware reset signal when the "3.3V" power supply voltage drops below 3.08 V.
The watchdog timer can be used to avoid software freeze-ups. The WDT0 and WDT1 watchdog timers are triggered in the absence of software confirmations for 30.5 µs ... 512 sec. The internal watchdog timer is started in the SYSTEM BIOS SETUP. It is possible to configure the actuation of the internal watchdog timer with or without generation of a hardware reset signal.
The device is reset when the power is turned on, by software, as well as by pressing the "RESET" button.

1.10.3 RAM

The device uses dynamic DDR3 SDRAM with a total size of 2 GB and operating at a frequency of 667 MHz as a system memory. The memory module cannot be expanded.

1.10.4 Non-volatile RAM

The device has 8 KB of integrated non-volatile RAM made by FRAM technology and does not require battery power. The SPI interface of the processor is used to access the non-volatile memory.

1.10.5 Read Only Memory (FLASH BIOS)

For storing the basic input / output system (hereinafter referred to as BIOS), the device uses flash-memory chip of 2 MB, integrated into the Vortex86DX3 processor chip.

1.10.6 SATA port

The drive in SATA format may be connected to the device via the standard SATA connector. The SATA controller supports operation in the 1.5 Gb GenI and 3 Gb GenII modes. The power supply of the connected drive from the CPC314 module is not provided.
The connected SATA drive within the system is defined as the Secondary IDE Master.

1.10.7 Slot for microSD cards

The drive in the microSD format with a size of no less than 4GB and designed for industrial ambient temperature range is installed into microSD (XS4) slot when delivered. Type of the NAND Flash memory used: pSLC.
The connected microSD drive is defined within the system as the Primary IDE Master.

1.10.8 COM1- COM4 serial ports

The device controller has 4 x asynchronous serial ports:

- **COM1, COM2 – RS-232 (9-wire interface, non-insulated);**
- **COM3, COM4 – RS-422/485 (3- or 5-wire connection, insulated 500 V).**

RS-232 COM1 (0x3F8h) and COM2 (0x2F8h) serial ports, as well as RS-422/485 COM3 (0x3E8h) and COM4 (0x2E8h) ports are implemented on the UART controllers integrated into the Vortex86DX3.

The COM1 (RS-232) port of the CPC314 module corresponds to the "serial port 5" of the Vortex86DX3 CPU, COM2 (RS-232) – "serial port 6", COM3 (RS-422/485) – "serial port 1", COM4 (RS-422/485) – "serial port 2".

COM3 (XP16) and COM4 (XP17) ports operate in the RS-422/485 mode and provide galvanic isolation up to 500 V (each port has individual isolation from the system). The maximum data transfer rate is 1.5 Mb/sec. The ports are routed to 5-pin B5B-PH-KL (JST) connectors. For manufacturing the cable, it is recommended to use a PHR-5 socket, JST with SPH-002T-P0.5S pins, JST (available for order as a set ACS00031-01) and a shielded twisted pair or a ribbon cable.

Table 1-3 – Purpose of the pins of RS-422/485 (XP16, XP17) ports

COM3-4: B5B-PH-KL (JST)		
Pin #	**Function (RS-422)**	**Function (RS-485)**
1	TX+	RTxD+
2	TX-	RTxD-
3	RX+	-
4	RX-	-
5	GNDS	GNDS

The “GNDS” circuit corresponds to the signal isolated “ground” of the interface, the GNDS circuits of the different ports are isolated from each other and are not interconnected.
By setting the X4, X5 (COM3) and X6, X7 (COM4) jumpers, the matching circuits are connected to the signal lines of the RS-422 or RS-485 interfaces and the operating mode is set.
For port operation in the RS-485 mode it is necessary to connect the "TX+" with "RX+" lines and "TX-" with "RX-" lines.

Attention!
For proper operation of RS-422/485 transmit/receive unit in a multiuser network, use the appropriate jumpers to install 120 Ohm terminators at the 2 most distant network nodes, as well as the 680 Ohm biasing resistors (at one or two of the most distant network nodes).

Table 1-4 – Configuration of the COM3 (X4, X5) port

Jumper	**Description**
X4[1-2] [5]	Biasing resistor is set on the line TX+
X5[1-2]	Biasing resistor is set on the line TX-
X4 and X5	120 Ohm matching resistor is connected to the TX+ / TX-

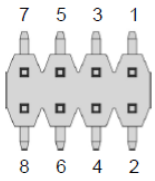
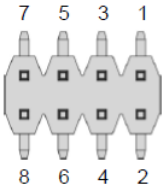


Table 1-5 – Configuration of the COM4 (X6, X7) port

Jumper	**Description**
X6[1-2] [6]	Biasing resistor is set on the line TX+
X7[1-2]	Biasing resistor is set on the line TX-
X6 and X7	120 Ohm matching resistor is connected to the TX+ / TX-



Each port contains lightning protection circuits based on protection elements of TBU series and TISP series thyristor protection circuits. The port also contains TVS diode-based pulse interference protection circuits. The diagram of the output stages of the COM3 port is shown below (the COM4 port has a similar circuit design).

[5] The position of the switches at the time of delivery is highlighted in bold; if none is highlighted, the switches are not set at delivery.
[6] The position of the switches at the time of delivery is highlighted in bold; if none is highlighted, the switches are not set at delivery.

The maximum number of modules connected to the RS-485 network together with the device amounts to 64, provided that the input impedance of the RS-485 drivers is at least 96 kOhm.

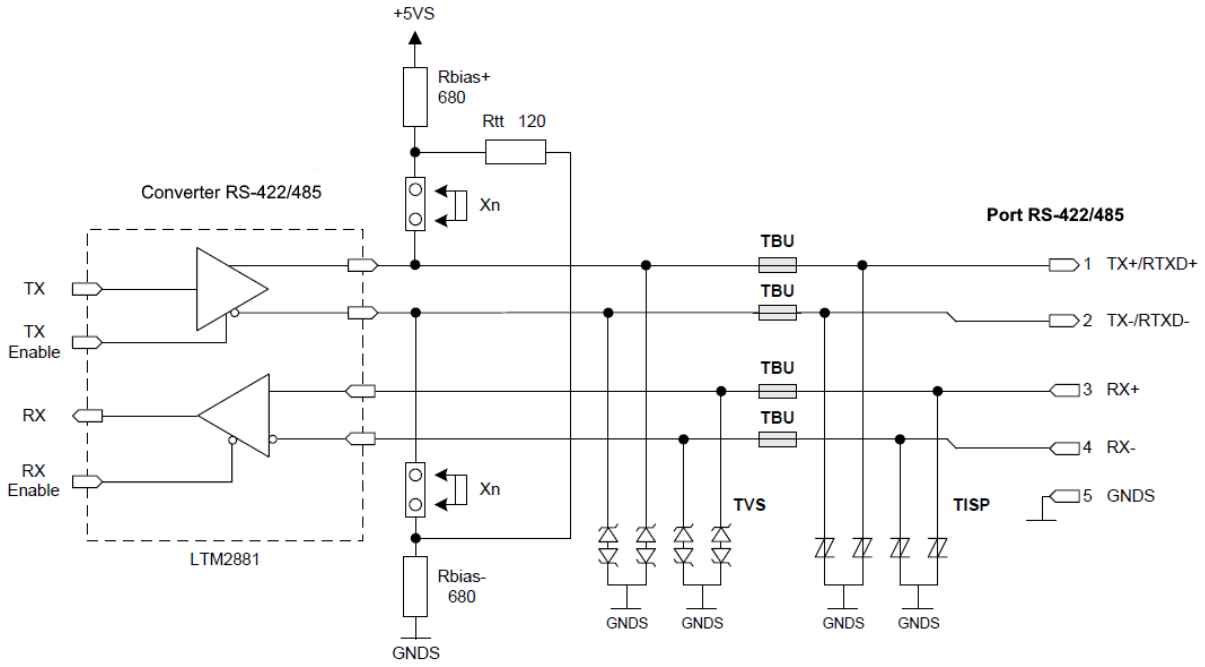


Fig. 1-5 – Output stages of RS-422/485 ports of the device

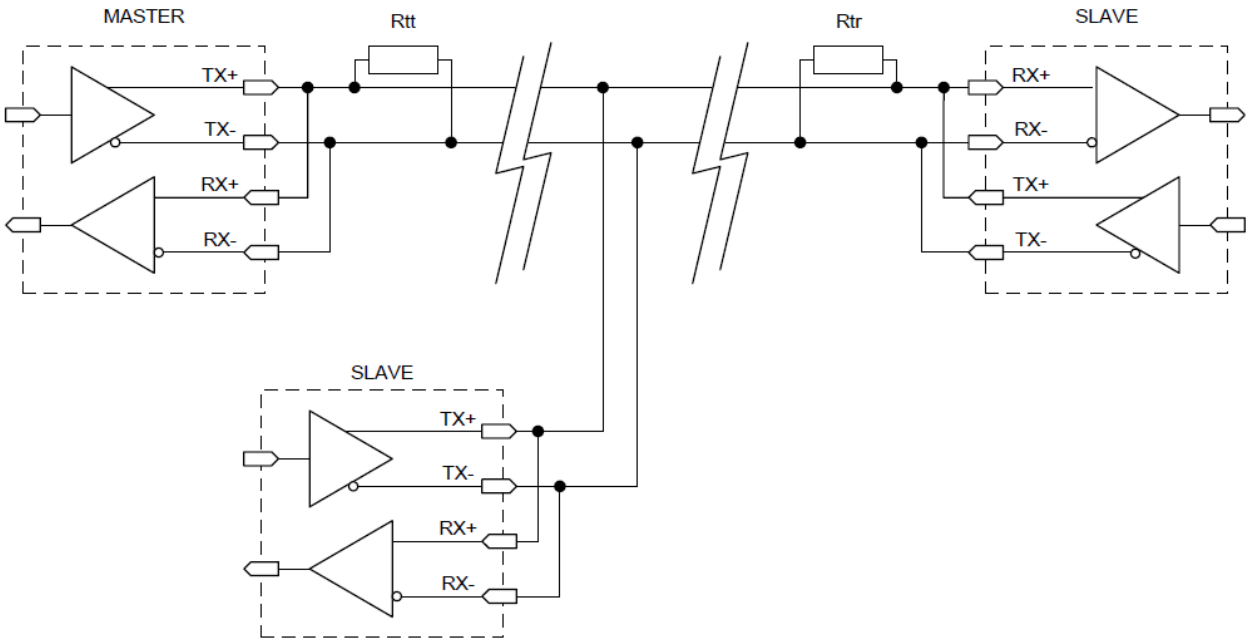


Fig. 1-6 – Connecting modules via RS-485 interface

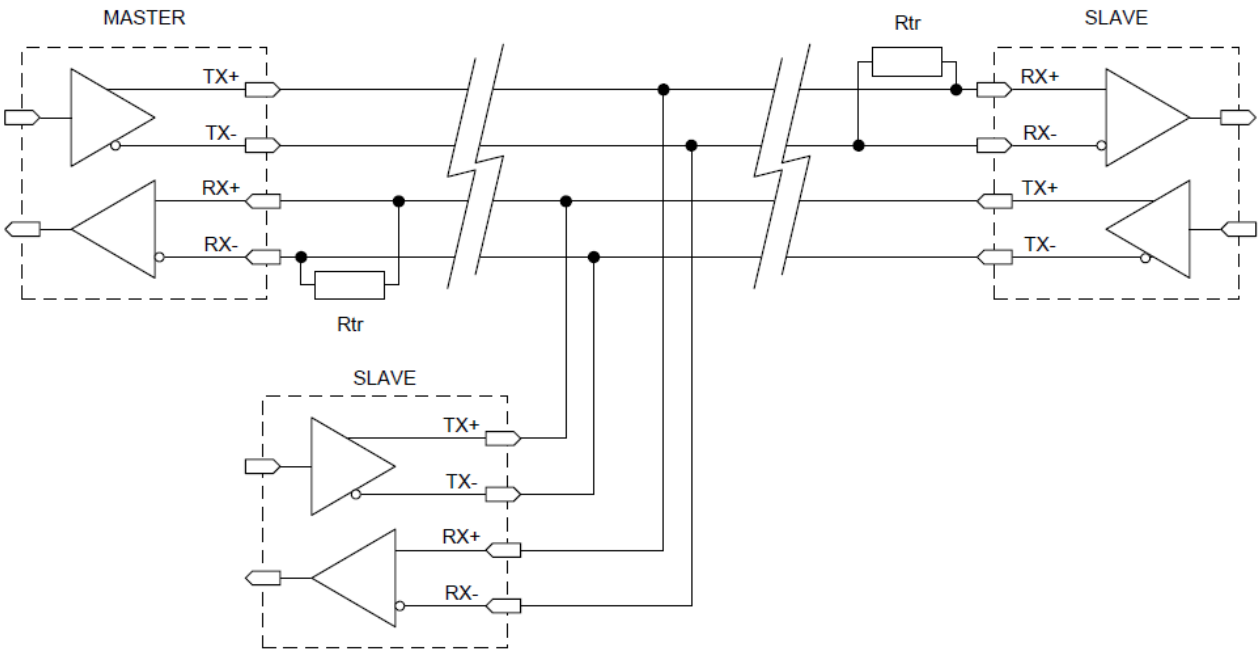


Fig. 1-7 – Connecting modules via RS-422 interface

The COM1 (XP14) and COM2 (XP15) ports operate in RS-232 mode. The maximum data exchange rate for COM1 and COM2 is 230,400 bit/s. The ports are fully software compatible with the 16550 UART model.
Each port is routed to a vertical two-row 10-pin connector of the IDC2-10 type with a pitch of 2 mm (98414-G06-10LF, FCI). As a mating part, it is necessary to use a 10-pin socket 89947-710LF (FCI) for a ribbon cable with a pitch of 1 mm. A ready-made cable (IDC2-10 - DB9M) ACS00023-04 is available for ordering, cable length: 17 cm.
The both ports can be used for console I/O and file downloads. A null-modem cable is required to communicate with a PC used as a hyperterminal.
By default, the console port is COM1 (port settings in the terminal program PuTTY, Hyperterminal: rate – 115,200 bit/s, data bit - 8, stop bit - 1, no parity check).

Table 1-6 – Purpose of the pins of RS-232 (XP14, XP15) ports

COM1, COM2: 98414-G06-10LF (FCI)			
Pin#	**Function**	**Pin#**	**Function**
1	DCD	2	DSR
3	RXD#	4	RTS
5	TXD#	6	CTS
7	DTR	8	RI
9	GND	10	+5V_EXTR

The base addresses and interrupts for serial ports are set in BIOS Setup. By default, the following base addresses/interrupts are set for serial ports in BIOS Setup:

COM1 (RS-232): 0x3F8 / IRQ4, [115200 8,n,1] [7]
COM2 (RS-232): 0x2F8 / IRQ3, [115200 8,n,1]
COM3 (RS-485): 0x3E8 / IRQ4, [115200 8,n,1]
COM4 (RS-485): 0x2E8 / IRQ3, [115200 8,n,1]
The exchange rate for serial ports can be set in the BIOS Setup. The exchange rate is determined by the value of the CPU frequency divider register. The value of the divider and the data exchange rate is calculated using the following formulas:

DIV = F / (16 • BR), BR=F / (DIV • SM))

- F – internal generator frequency, MHz (F = 1.8432 / 24 / 48);
- DIV (divider) – divider value (for F = 1.8432, 24 and 48 MHz – minimum value DIV = 1);
- BR (baud rate) - required exchange rate, bit/sec;
- SM (sampling mode) – Base divider value (SM = 16).

Attention!
The receiver allows the exchange rate value downward bias by 3.0% and upward bias by 2.5%.

Table 1-7 – Frequency divider values for serial ports

Exchange rate, bit/s	F=1.8432 MHz		F=24 MHz		F=48 MHz	
	Divider	Error, %	Divider	Error, %	Divider	Error, %
300	384	–	5000	–	10000	–
600	192	–	2500	–	5000	–
1200	96	–	1250	–	2500	–
2400	48	–	625	–	1250	–
3600	32	–	417	–	625	–
4800	24	–	312	–	625	–
7200	16	–	208	–	417	–
9600	12	–	156	–	312	–
19200	6	–	78	–	156	–
38400	3	–	39	–	78	–
57600	2	–	26	–	52	–
115200	1	–	13	–	26	–
200000	–	–	–	–	–	–
230400	–	–	–	–	13	–
250000	–	–	6	–	12	–
300000	–	–	5	–	10	–
460800	–	–	–	–	–	–
1 500 000	–	–	1	–	2	–

[7] The exchange rate is 115,200 bit/s, 8 bits, no parity check, 1 stop bit

1.10.9 PS/2 keyboard / mouse port

Interface for connection of PS/2-keyboard and mouse is routed to 6-pin XP8 connector (B6B-PH-KL, JST).
To manufacture the cable, using PHR-6 socket, JST with pins SPH-002T-P0.5S, JST (available for ordering as a ACS00031-02 set) is recommended. A ready-made adapter for connecting a PS/2 keyboard/mouse with a length of 200 mm is available to order as ACS00043. To connect a mouse, you should additionally use a standard Y-cable.

Table 1-8 – Purpose of pins of PS/2 (XP8) port

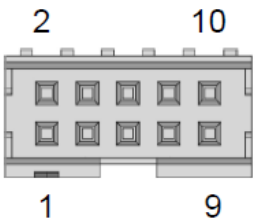
PS/2: B6B-PH-KL (JST)	
Pin#	**Function**
1	KBD_CLK
2	KBD_DAT
3	MS_CLK
4	GND
5	+5V_EXTK
6	MS_DAT

1.10.10 USB1, USB2 ports

The Device Controller has 2 x USB Host ports supporting USB 1.1 and USB 2.0 specifications. The operating mode of the interfaces is set in the BIOS Setup menu.
Each of the channels has an independent power supply control circuit and power protection (+5 V, 500 mA).
The USB ports are routed to one XP3 connector: IDC2-20, 10-pin, two-row male connector with a pitch of 2 mm, 98414-G06-10LF (FCI).
A 10-pin socket 89947-710LF (FCI) to a flat ribbon cable with a pitch of 1 mm or a 10-pin socket 10073599-010LF (FCI) with pins 77138-101LF (FCI) should be used as a mating part.
A 200mm USB device adapter is available for ordering as ACS00051-01.

Table 1-9 – Purpose of pins of the USB (XP3) ports

USB1-2: 98414-G06-10LF (FCI)			
Pin #	**Function**	**Pin #**	**Function**
1	+5 V @ 0.5A	2	+5 V @ 0.5A
3	D-	4	D-
5	D+	6	D+
7	GND	8	GND
9	GND	10	GND

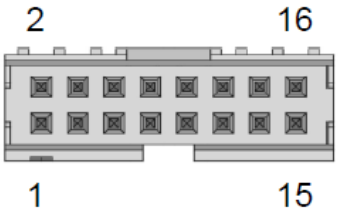


1.10.11 LAN1, LAN2 ports

The device contains 2 x LAN ports.
LAN1 port supports 10/100 Mbit/s operation modes and is based on Intel WGI210IT controller. The LAN2 port supports 10/100 Mbit operation modes and is implemented on the basis of a controller built into the Vortex86DX3 microprocessor.
The ports provide galvanic isolation up to 500 V (each port is individually isolated from the system).
The LAN ports are routed to a single XP1 connector: IDC2-16, 16-pin two-row
Each port is routed to a two-row 10-pin connector with a pitch of 2 mm, 98414-G06-10LF (FCI). 10-pin socket 89947-710LF (FCI) for a flat ribbon cable with a pitch of 1 mm or a 10-pin socket 10073599-010LF (FCI) with pins 77138-101LF (FCI).

Table 1-10 – Purpose of pins of the LAN1, LAN2 (XP1) ports

LAN1, LAN2: 98414-G06-16LF (FCI)			
Pin #	**Function**	**Pin #**	**Function**
1	LAN1 TX+	2	LAN1 TX-
3	LAN1 RX+	4	-
5	-	6	LAN1 RX-
7	-	8	-
9	LAN2 TX+	10	LAN2 TX-
11	LAN2 RX+	12	-
13	-	14	LAN2 RX-
15	-	16	-



1.10.12 RTC, SPI FRAM, lithium battery

The device is equipped with an AT-compatible real-time clock with an installed CR2032 lithium battery with a capacity of 200 mAh. The battery is installed into the XS3 socket located on the back of the board. Battery service life is decreased at high and low ambient temperatures, in case of a high degree of contamination of the module's PCB, as well as when the module is in the off state for a long time. The average service life is 4 to 10 years.

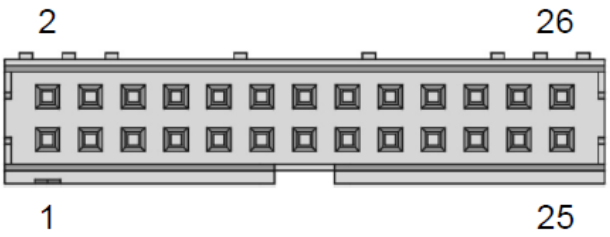
Important note!
If the device is turned off for a long time, it is recommended to synchronize the real-time clock with the exact time readings.
FRAM nonvolatile memory with the serial SPI interface is designed to save the SETUP BIOS copy and restore the RTC memory state in case of an error.

1.10.13 LPT port

The universal parallel port with support for SPP (PC-compatible printer port), EPP (Extended Capabilities Port) and ECP (Enhanced Parallel Port) modes.
The LPT port is routed to XP5 connector: IDC2-26, 26-pin, double-row male connector with a pitch of 2 mm, 98424-G52-26LF (FCI).
As a mating part, you should use a 26-pin socket 89947-726LF (FCI) for a ribbon cable with a pitch of 1 mm or a 26-pin socket 10073599-026LF (FCI) with the 77138-101LF (FCI) pins.

Table 1-11 – Purpose of pins of LPT (XP5) connector

LPT: 98424-G52-26LF (FCI)				
Pin #	**Function**		**Pin #**	**Function**
1	STB#		2	AFD#
3	PD0		4	ERR#
5	PD1		6	INIT#
7	PD2		8	SLCTIN#
9	PD3		10	GND
11	PD4		12	GND
13	PD5		14	GND
15	PD6		16	GND
17	PD7		18	GND
19	ACK#		20	GND
21	BUSY		22	GND
23	PE		24	GND
25	SLCT#		26	+5V_EXTP



1.10.14 VGA and LVDS ports

The video subsystem of the device is based on a video processor integrated into the Vortex86DX3 processor. The video controller with a 2D accelerator function has the following technical specifications and capabilities:

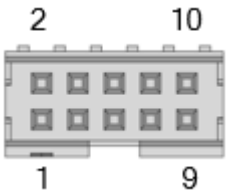
- video memory size – to be allocated from the system memory;
- possibility to connect RGB (VGA) monitors with max. resolution of 1920 x 1440 (60 Hz, 32 bit);
- possibility to connect LVDS panels with max. resolution of 1920 x 1440 (60 Hz, 32 bit)[8].

The VGA is routed to the XP12 connector: IDC2-10, two-row 10-pin male connector with a pitch of 2 mm, 98414-G06-10LF (FCI).
As a mating part, you should use a 10-pin 89947-710LF (FCI) socket for a ribbon cable with a pitch of 1 mm or a 10-pin 10073599-010LF (FCI) socket with the 77138-101LF (FCI) pins. A ready-made cable (IDC2-10 - DB15F) ACS00027-02 is available for order, with a length of 17 cm.

[8] In the event of connecting both VGA monitor and LVDS panel, their maximum resolution would be 1280 x 1024.

Table 1-12 – Purpose of the VGA (XP12) port pins

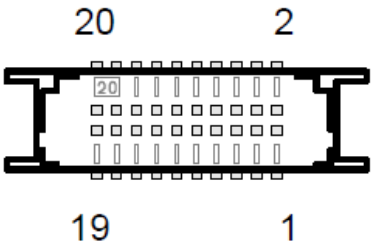
VGA: 98414-G06-10LF (FCI)			
Pin #	**Function**	**Pin #**	**Function**
1	RED	2	GND
3	GREEN	4	GND
5	BLUE	6	GND
7	HSYNC	8	VSYNC
9	DDC_SCL	10	DDC_SDA



The LVDS port is routed to the XP13 connector: IDC2-26, two-row 20-pin connector with a pitch of 1.25 mm, DF13EA-20DP-1.25V (Hirose).
As a mating part, you should use the 20-pin DF13-20DS-1.25C (Hirose) socket with DF13-2630SCF (Hirose) pins.

Table 1-13 – Purpose of LVDS (XP13) port pins

LVDS: DF13EA-20DP-1.25V (Hirose)			
Pin #	**Function**	**Pin #**	**Function**
1	VCC (+3.3 V)	2	VCC (+3.3 V)
3	DATA0+	4	DATA0-
5	GND	6	GND
7	DATA1+	8	DATA1-
9	GND	10	GND
11	DATA2+	12	DATA2-
13	GND	14	GND
15	DATA3+	16	DATA3-
17	GND	18	GND
19	CLK+	20	CLK-



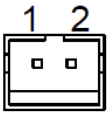
1.10.15 Audio ports

The device's audio ports are based on the HDA audio controller integrated into the Vortex86DX3 microprocessor and the CS4207 24-bit audio codec (Cirrus Logic).
The codec is compatible with the SBPRO™ model.
The set of audio ports includes: an audio output (STEREO) and a MIC (STEREO).
The DAC2 (LINE-OUT) output is used as audio output and ADC1 of the CS4207 audio codec is used as audio input.
LINE-IN and LINE-OUT audio input and output are routed to 5-pin XP10 (B5B-PH-KL, JST) connector. MIC-IN microphone input is routed to the 2-pin XP11 (B2B-PH-KL, JST) connector.
For manufacturing the cable it is recommended to use PHR-5 and PHR-2 sockets, JST socket with SPH-002T-P0.5S, JST pins (available for order as ACS00031-01 and ACS00031-03 sets).

Table 1-14 – Purpose of Audio ports pins (XP10, XP11)

LINE IN/OUT: B5B-PH-KL (JST)	
Pin#	**Function**
1	LINE-IN_L
2	LINE-IN_R
3	GND
4	LINE-OUT_R
5	LINE-OUT_L

MIC: B2B-PH-KL (JST)	
Pin#	**Function**
1	MIC-IN
2	GND



1.10.16 PC/104 expansion bus (ISA 8/16-bit)

The PC/104 (XS1) connector is designed for installing expansion modules of the PC/104 or PC/104-plus format to the module. It is allowed to install no more than 4x PC/104 expansion modules.

ISA bus operating modes: 8/16 bit, 8.3/16.6 MHz. Master Mode is not supported.

The device is equipped with an AMP 1375795-5 connector (pins B10 and C19 are missing) and an AMP 1445251-1 organizer.

Table 1-15 – Purpose of XS1 connector pins: PC/104 (ISA 8/16-bit) rows A, B

ISA: Connector of PC/104 expansion bus (2x32 + 2x20 pins), rows A, B					
Pin #	**Purpose**	**Configuration**	**Pin #**	**Purpose**	**Configuration**
A1	IOCHK#	Input	B1	GND	Power supply
A2	SD7	Input/Output	B2	RESET	Output
A3	SD6	Input/Output	B3	+5V	Input
A4	SD5	Input/Output	B4	IRQ9	Input
A5	SD4	Input/Output	B5	-	
A6	SD3	Input/Output	B6	DRQ2	Input
A7	SD2	Input/Output	B7	-12V	Power supply
A8	SD1	Input/Output	B8	0WS#	Input
A9	SD0	Input/Output	B9	+12V	Power supply
A10	IOCHRDY	Input	B10	GND	Power supply
A11	AEN	Output	B11	SMEMW#	Output
A12	SA19	Output	B12	SMEMR#	Output
A13	SA18	Output	B13	IOW#	Output
A14	SA17	Output	B14	IOR#	Output
A15	SA16	Output	B15	DACK3#	Output
A16	SA15	Output	B16	DRQ3	Input
A17	SA14	Output	B17	DACK1#	Output

A18	SA13	Output		B18	DRQ1	Input
A19	SA12	Output		B19	DACK0#	Output
A20	SA11	Output		B20	BCLK	Output
A21	SA10	Output		B21	IRQ7	Input
A22	SA9	Output		B22	IRQ6	Input
A23	SA8	Output		B23	IRQ5	Input
A24	SA7	Output		B24	IRQ4	Input
A25	SA6	Output		B25	IRQ3	Input
A26	SA5	Output		B26	DACK2#	Output
A27	SA4	Output		B27	TC	Output
A28	SA3	Output		B28	BALE#	Output
A29	SA2	Output		B29	+5V	Power supply
A30	SA1	Output		B30	OSC	Output
A31	SA0	Output		B31	GND	Power supply
A32	GND	Power supply		B32	GND	Power supply

Table 1-16 - Purpose of XS1 connector pins: PC/104 (ISA 8/16-bit) rows C, D

ISA: Connector of PC/104 bus expansion (2x32 + 2x20 pins), rows C, D						
Pin #	**Purpose**	**Configuration**		**Pin #**	**Purpose**	**Configuration**
C0	GND	Power supply		D0	GND	Power supply
C1	SBHE#	Output		D1	MEMCS16#	Input
C2	LA23	Output		D2	IOCS16#	Input
C3	LA22	Output		D3	IRQ10	Input
C4	LA21	Output		D4	IRQ11	Input
C5	LA20	Output		D5	IRQ12	Input
C6	LA19	Output		D6	IRQ15	Input
C7	LA18	Output		D7	IRQ14	Input
C8	LA17	Output		D8	DACK0#	Output
C9	MEMR#	Output		D9	DRQ0	Input
C10	MEMW#	Output		D10	DACK5#	Output
C11	SD8	Input/Output		D11	DRQ5	Input
C12	SD9	Input/Output		D12	DACK6#	Output
C13	SD10	Input/Output		D13	DRQ6	Input
C14	SD11	Input/Output		D14	DACK7#	Output
C15	SD12	Input/Output		D15	DRQ7	Input
C16	SD13	Input/Output		D16	+5V	Power supply
C17	SD14	Input/Output		D17	-	
C18	SD15	Input/Output		D18	GND	Power supply
C19	-			D19	GND	Power supply

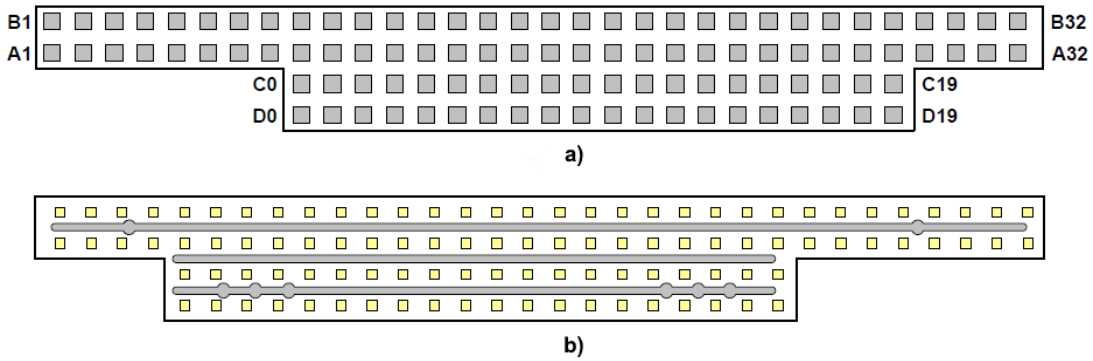


Fig. 1-8 – Numbering pins of the XS1 connector a) top view of the device, b) bottom view of the device with the organizer installed into connector

1.10.17 PC/104-plus expansion bus (PCI 32-bit)

The device can be connected to 3 x expansion boards of the PC/104-plus or PCI/104 format. The PCI104 bus (PCI, 32 bit, 33 MHz) supports up to 3 x PCI master devices.
The interface is routed to the XS2 connector (PCI/104 connector, 120 pins, 2 mm pitch).
The product has an AMP 1375799-1 connector and an AMP 1375801-1 organizer.

Table 1-17 – Purpose of XS2 connector pins: PCI/104 (PCU 32-bit) rows A, B

PCI: Connector of PCI/104 bus expansion (4x30 pins), rows A, B					
Pin #	**Purpose**	**Configuration**	**Pin #**	**Purpose**	**Configuration**
A1	GND	Power supply	B1	-	-
A2	VI/O	+3.3V (output)	B2	AD2	I/O
A3	AD5	I/O	B3	GND	Power supply
A4	C/BE0#	I/O	B4	AD7	I/O
A5	GND	Power supply	B5	AD9	I/O
A6	AD11	I/O	B6	VI/O	+3.3V (output)
A7	AD14	I/O	B7	AD13	I/O
A8	-	-	B8	C/BE1#	I/O
A9	SERR#	PU (10K)	B9	GND	Power supply
A10	GND	Power supply	B10	PERR#	PU (10K)
A11	STOP#	I/O	B11	-	-
A12	-	-	B12	TRDY#	I/O
A13	FRAME#	I/O	B13	GND	
A14	GND	Power supply	B14	AD16	I/O
A15	AD18	I/O	B15	-	-
A16	AD21	I/O	B16	AD20	I/O
A17	-	-	B17	AD23	I/O
A18	IDSEL0	AD12	B18	GND	Power supply
A19	AD24	I/O	B19	C/BE3#	I/O
A20	GND	Power supply	B20	AD26	I/O
A21	AD29	I/O	B21	+5V	Power supply
A22	+5V	Power supply	B22	AD30	I/O

PCI: Connector for expansion of PCI/104 bus (4x30 pins), rows A, B					
Pin #	**Purpose**	**Configuration**	**Pin #**	**Purpose**	**Configuration**
A23	REQ0#	Input	B23	GND	Power supply
A24	GND	Power supply	B24	REQ2#	Input
A25	GNT1	Output	B25	VI/O	+3.3V (output)
A26	+5V	Power supply	B26	CLK0	Output
A27	CLK2	Output	B27	+5V	Input
A28	GND	Power supply	B28	INTD#	Input
A29	+12V	-	B29	INTA#	Input
A30	-	-	B30	REQ3#	Input

Table 1-18 – Purpose of XS2 connector pins: PCI/104 (PCU 32-bit) rows C, D

PCI: Connector of PCI/104 bus expansion (4x30 pins), rows C, D					
Pin #	**Purpose**	**Configuration**	**Pin #**	**Purpose**	**Configuration**
C1	+5V	Power supply	D1	AD0	I/O
C2	AD1	I/O	D2	+5V	Power supply
C3	AD4	I/O	D3	AD3	I/O
C4	GND	Power supply	D4	AD6	I/O
C5	AD8	I/O	D5	GND	Power supply
C6	AD10	I/O	D6	M66EN (GND)	
C7	GND	Power supply	D7	AD12	I/O
C8	AD15	I/O	D8	-	-
C9	-	-	D9	PAR	I/O
C10	-	-	D10	-	-
C11	LOCK#	PU (10K)	D11	GND	Power supply
C12	GND	Power supply	D12	DEVSEL#	I/O.
C13	IRDY#	I/O	D13	-	-
C14	-	-	D14	C/BE2#	I/O
C15	AD17	I/O	D15	GND	Power supply
C16	GND	Power supply	D16	AD19	I/O
C17	AD22	I/O	D17	-	-
C18	IDSEL1	AD13	D18	IDSEL2	AD14
C19	VI/O	+3.3V (output)	D19	IDSEL3	AD15
C20	AD25	I/O	D20	GND	Power supply
C21	AD28	I/O	D21	AD27	I/O
C22	GND	Power supply	D22	AD31	I/O
C23	REQ1#	Input	D23	VI/O	+3.3V (output)
C24	+5V	Power supply	D24	GNT0#	Output
C25	GNT2#	Output	D25	GND	Power supply
C26	GND	Power supply	D26	CLK1	Output
C27	CLK3	Output	D27	GND	Power supply

C28	+5V	Power supply	D28	RST#	Output
C29	INTB#	Input	D29	INTC#	Input
C30	GNT3#	Output	D30	GND	Power supply

The “Status” column indicates the direction of data transmission for the case when the device is the bus master.

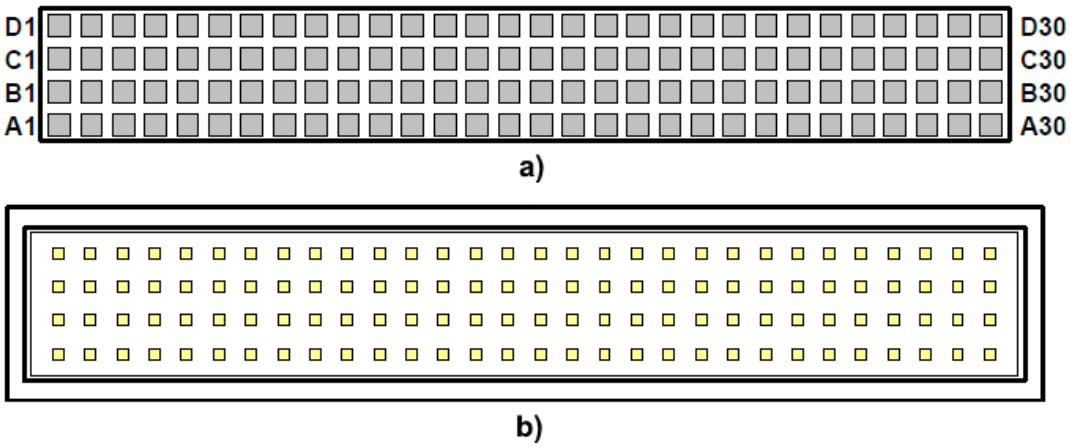


Fig. 1-9 – Numbering XS2 connector pins a) top view of the device, b) bottom view of the device with the organizer installed into connector

1.10.18 Diagnostic LEDs and XP9 connector

All the LEDs are located on the top side of the device. The purpose of the LEDs is shown in Table 1-23.

Table 1-19 – Purpose of device LEDs

LED	Function
HL1 (red)	Indication of short circuit or voltage output of one of the module’s secondary power supplies outside the working range
HL1 (green)	Indication of the state of the input supply voltage +5 V
HL2 (red)	Indication of the hardware reset
HL3 (green)	Indication of LAN1 activity
HL4 (green)	Indication of LAN2 activity
HL5 (red)	User LED, GPIO_P7[0] port
HL5 (green)	User LED, GPIO_P7[1] port

XP9 male connector is provided for relocating indication from the board.

Table 1-20 – Purpose of pins of XP9 indication connector

Connector pins	Function
XP9[1-2]	Indication of the state of input power supply voltage +5 V
XP9[3-4]	Indication of hardware reset
XP9[5-6]	Indication of LAN1 activity
XP9[7-8]	Indication of LAN2 activity
XP9[9-10]	User LED, GPIO_P7[0] port
XP9[11-12]	User LED, GPIO_P7[1] port
* Even pins correspond to the cathode "-", odd pins – to the anode "+" for connection of LED.	

1.10.19 Sensors

The device is equipped with the TMP75AIDR (National Semiconductor) temperature sensor, which makes it possible to measure the temperature on the product surface with a resolution of 12 bits within the range from -55 to +125 °C, supplementary code with the sign. The sensor is located on the board in the area of the Vortex86DX3 processor. The temperature sensor is connected to the I2C0 bus of the processor. Address on the I2C bus: write - 0x90, read - 0x91 (the most significant seven bits of the address: b'1001000 + the least significant bit: b'0 for writing, b'1 for reading). The TMP75AIDR sensor allows you to monitor the temperature of the module in the processor area. The measurement error is not standardized, the typical error is determined by the characteristics declared by the sensor manufacturers.
To use the sensor as a measuring one, such a sensor should be calibrated (the system that stores calibration factors can be arranged on the basis of FRAM non-volatile memory).
An example of sensor programming is given in subparagraph **4.9 "Working with I2C Devices"**.

1.10.20 Measuring the device's power supply voltages

To measure the secondary power supply voltages of the device, an analog-to-digital converter integrated into the Vortex86DX3 is used. The measurement error is not standardized, the typical error is determined by the characteristics declared by the Vortex86DX3 processor manufacturer. The relevant table below shows how the lines of the ADC_AUX [7: 0] port match the secondary supply voltages of the device.

Table 1-21 – Purpose of ADC channels ADC_AUX [7:0]

ADC_AUX port	Power supply voltage
ADC_AUX [0]	+5 V (main supply voltage) at the input a voltage divider ½ is installed (implemented on 2 x 1 kOhm resistors, 1%)
ADC_AUX [1]	+3.3 V (supply voltage used to start the secondary converters: 0.95, 1.2, 1.35, 1.8, 3.3 V)
ADC_AUX [2]	+0.95 V (CPU core voltage)
ADC_AUX [3]	+1.2 V (PCIe, SATA supply voltage)
ADC_AUX [4]	+1.35 V (DDR3 supply voltage)
ADC_AUX [5]	+1.8 V (GPU, PLL, ANALOG supply voltage)
ADC_AUX [6]	+3.3 V (supply voltage of GPIO, ISA ports and other I/O ports)
ADC_AUX [7]	0 V

1.10.21 GPIO port

The GPIO port of the module is based on the GPIO_P2 [7: 0] port of the Vortex86DX3 processor. The port lines are tolerant towards the 5V voltage level. Each port line can be configured as input or output. The par value of the pull-up resistor for each line is 10 kOhm.

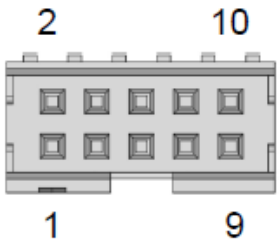
To ensure the accuracy of the state of the GPIO port lines after power-up, it is recommended to use a dedicated supply voltage line (+ 5VEXT, output No. 9 of XP2 connector) to power the logic connected to the GPIO port, and also use a high (+5 V) or low (GND) levels directly in devices connected to the port. When connecting external devices, the common wire connection (XP2 connector, output 10) is mandatory.

The GPIO port is routed to the XP2 connector (98414-G06-10LF, FCI).

To make a cable for the GPIO port, it is recommended to use a 10-pin socket per flat ribbon cable with a pitch of 1 mm: 89947-710LF (FCI).

Table 1-22 – Purpose of GPIO (XP2) port pins

GPIO: 98414-G06-10LF (FCI)			
Pin #	**Function**	**Pin #**	**Function**
1	GPIO (0)	2	GPIO (1)
3	GPIO (2)	4	GPIO (3)
5	GPIO (4)	6	GPIO (5)
7	GPIO (6)	8	GPIO (7)
9	+5VEXT	10	GND



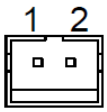
1.10.22 Isolated Remote Reset Port

The hardware reset port of the module is based on the GPIO_P2 [7: 0] port of the Vortex86DX3 processor.

To receive a reset signal using the XP18 connector, feed the voltage to the XP18/1 and XP18/2 connector pins ranging from + 3 to 5.5 V.
To manufacture the cable, it is recommended to use a PHR-2 (JST) socket with SPH-002T-P0.5S (JST) pins.

Table 1-23 – Purpose of GPIO (XP18) port pins

RESET: B 2B-PH-KL (JST)			
Pin #	**Function**	**Pin #**	**Function**
1	+V (+3…+5.5 V)	2	GND

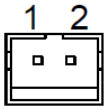


1.10.23 Port for External Battery Connection

To connect an external battery, you should use XP6 2-pin connector.
To manufacture the cable, it is recommended to use a PHR-2 (JST) socket with SPH-002T-P0.5S (JST) pins. Voltage range: from +2.9 to 3.3 V.

Table 1-24 – Purpose of GPIO (XP6) port pins

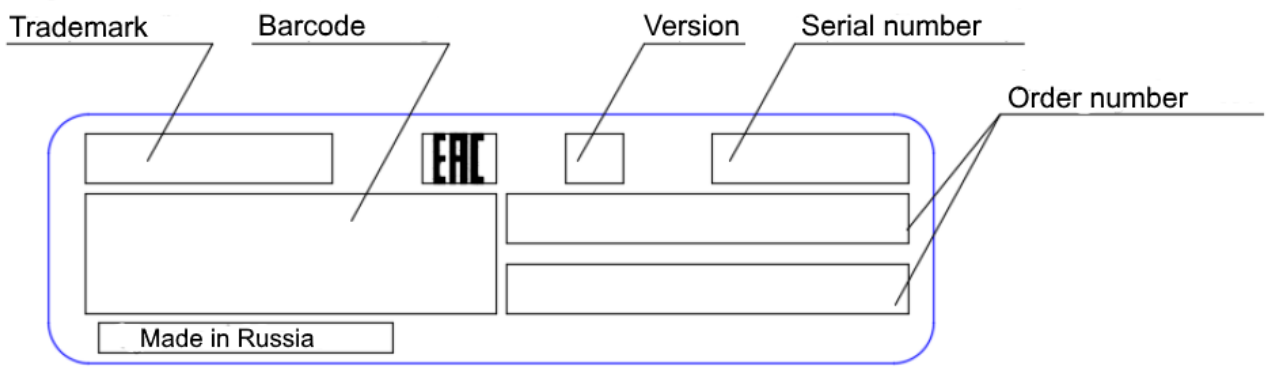
3V BATTERY: B 2B-PH-KL (JST)			
Pin #	**Function**	**Pin #**	**Function**
1	+3 V	2	GND



1.11 Labelling

The consumer container used for storing the product is labelled by means of an individual identifier (sticker).
The consumer container sticker contains the following information:

Product designation;
Device version;
Serial number of the device;
Manufacturer’s trademark;
Barcode.



** The location of the fields with product-related information may differ slightly from the one shown in this figure.*

1.12 Packaging

The product is packed in individual antistatic packaging (bag) with the following dimensions: 152 x 254 mm and placed in a separate consumer container (cardboard box). The box dimensions are: 155 x 140 x 45 mm.

Note

Retain the original packaging for storing products in the future or to transport in case of a warranty claim. If it is necessary to transport or store the board, pack it the same way as it was packed at the time of receipt.

2 Intended Use

2.1 Operating limitations

The safety requirements listed at the beginning of this User Manual should be strictly observed. Installation and removal of the device, connection to the slots should be carried out only with the power supply turned off. Always observe the proper orientation of the device connectors during installation.

Operation of the device where the supply voltage that does not correspond to the one specified in **subparagraph 1.4 Power supply** is not allowed.

Operation of the device when exposed to external factors that do not correspond to the ones specified in subparagraph 1**.2 Technical Specifications** is not allowed.

2.2 Distribution of hardware interrupts

Table 2-1 – Addresses of hardware interrupts

#	Default sources	Alternative sources
NMI		
IRQ0	*Reserved (system timer)*	
IRQ1	Keyboard	
IRQ2	Reserved (interrupt from the slave controller)	
IRQ3	COM2 / COM4	
IRQ4	COM1 / COM3	
IRQ5	USB	
IRQ6	Ethernet	
IRQ7	LPT port	
IRQ8	RTC (Real Time Clock)	
IRQ9	-	
IRQ10	Ethernet	
IRQ11	-	
IRQ12	-	
IRQ13	*Reserved (CPU support)*	
IRQ14	ATA controller	
IRQ15	-	

2.3 DMA channels

Table 2-2 – DMA channels of the device

#	Source
DRQ0	–

DRQ1	–
DRQ2	–
DRQ3	–
DRQ5	–
DRQ6	–
DRQ7	–

2.4 I/O address space

Table 2-3 – Distribution of I/O address space

Address	Function	Notes
–	–	–
0x7Ah	GPIO_P2 Data	Data register of GPIO_P2[7:0] port of the Vortex86DX3 processor
–	–	–
0x9Ah	GPIO_P2 Direction	Direction register of GPIO_P2[7:0] port of the Vortex86DX3 processor
–	–	–
0x179h	GPIO_P7 Data	Data register of GPIO_P7[7:0] port of the Vortex86DX3 processor
–	–	–
0x199h	GPIO_P7 Direction	Direction register of GPIO_P7[7:0] port of the Vortex86DX3 processor
–	–	–
0x2E8h – 0x2EFh	COM4	Serial port COM4, RS-485 (Serial Port 2, Vortex86DX3)
0x2F8h – 0x2FFh	COM2	Serial port COM2, RS-232 (Serial Port 6, Vortex86DX3)
–	–	–
0x378h – 0x37Ah	LPT	Parallel port
–	–	–
0x3E8h – 0x3EFh	COM3	Serial port COM3, RS-485 (Serial Port 1, Vortex86DX3)
0x3F8h – 0x3FFh	COM1	Serial port COM1, RS-232 (Serial Port 5, Vortex86DX3)
–	–	–

2.5 Memory address space

Table 2-4 – Addresses of memory devices

Address	Device	Notes
00000 – 9FFFFh	DOS	DOS Area 640 Kbyte
A0000 – BFFFFh	VGA	Video memory area 128 Kbyte
C0000 – C7FFFh	VGA BIOS	VGA BIOS 32 Kbyte
C8000 – DFFFFh	–	–
E0000 – EFFFFh	System BIOS	Extended System BIOS area 64 Kbyte (16 Kbyte x 4)
F0000 – FFFFFh	System BIOS	System BIOS area 64 Kbyte

Address	Device	Notes
10 0000 – MEMORY TOP *	DRAM	DDR3 SDRAM
MEMORY TOP * – FFE0 0000	PCI	PCI
FFE0 0000 – FFFF FFFFh	High BIOS	High BIOS Area 2 Mbyte (mapped to PCI)

* Installed DDR3 SDRAM – 2 GB.

2.6 Using the processor's GPIO ports

The Vortex86DX3 microchip has 10 x GPIO (General Purpose Input Output) I/O ports, available to the user through the internal registers of the microchip. Each port has 8 x I/O lines, each of which can be configured as input or output by programming the registers of the corresponding port.
For working with GPIO ports, 2 x 8-bit registers are used per port - a data register and a direction register. Each bit of the data register is mapped to the corresponding circuit on the board: bit 0 corresponds to the port 0 line (GPIO_Px0), bit 7 corresponds to the port 7 line (GPIO_Px7), etc.
Each bit of the direction register is mapped to the corresponding circuit on the board: bit 0 corresponds to the port 0 line (GPIO_Px0), bit 7 corresponds to the port 7 line (GPIO_Px7), etc.

Table 2-5 – GPIO control registers

	GPIO_P2	GPIO_P7	Description
Data register	0x7Ah	0x179h	
Direction register	0x9Ah	0x199h	0: Line is input 1: Line is output

Assigning the used GPIO ports is described in the table below.

Table 2-6 – Purpose of GPIO ports

I/O port line	I/O port line direction	Description
GPIO_P0 [7:0]	Input / Output	Reserved. The lines are used for COM1 port (RS-232).
GPIO_P1 [7:0]	Input / Output	Reserved. The lines are used for COM2 port (RS-232).
GPIO_P2 [7:0]	Input / Output	Reserved. GPIO port (XP2)
GPIO_P3 [3:0]	Input / Output	SPI interface. FRAM 64 Kb.
GPIO_P3 [5:4]	Input / Output	I2C0 interface. Temperature sensor.
GPIO_P3 [6]	Output	LVDS Shutdown Not used.
GPIO_P3 [7]	Output	LVDS PowerON Switching on the +3.3 V power supply of LVDS panel. Not used.
GPIO_P4 [7:0]	Input / Output	Serial port serial 1 of the processor (RS-422/485, COM3).
GPIO_P5 [7:0]	Input / Output	Serial port serial 2 of the processor (RS-422/485, COM4).
GPIO_P6 [7:0]	Input / Output	SD0 port. Connection of microSD card.
GPIO_P7 [0]	Output	Control of HL5 LED (red), active level ‘0’.
GPIO_P7 [1]	Output	Control of HL5 LED (green), active level ‘0’.
GPIO_P7 [2]	Input	Short circuit flag over USB ports. Active level '0'.
GPIO_P7 [3]	Input	Short circuit flag over +3.3V voltage connected to the PCI/104 (PCI bus 32 bit). Active level '0'.
GPIO_P7 [4]	Input	3V lithium battery low flag. Active level '0'.
GPIO_P7 [5]	Input	External opto-isolated reset / interrupt. Active level '0'. Triggered in case of the voltage on XP18 connector from 3 to 5.5 V.
GPIO_P7 [6]	Input	Resetting BIOS Setup settings by closing jumper X1. Active level '0'.
GPIO_P7 [7]	Input	User switch X2. Active level '0'.
GPIO_P8[7:0]	Input /	LPT port

GPIO_P9[8:0]	Output	LPT port
GPIO_PA[0]	Output	HDA controller reset (10k PULLDOWN).
GPIO_PA[4:1]	Input / Output	HAD interface (audio)
GPIO_PA[5]		LPT port
GPIO_PA[6]	Output	COM1_TXEN (output). RS-485 transmitter/receiver control signal, serial 1 port of the processor (RS-422/485).
GPIO_PA[7]	Output	COM2_TXEN (output). RS-485 transmitter/receiver control signal, serial 2 port of the processor (RS-422/485).
G_GPIO[2]		10k PULLDOWN.
G_GPIO[3]		10k PULLDOWN.

2.7 WDT0 and WDT1 watchdog timers

The Vortex86DX3 CPU chip has 2 x configurable hardware watchdog timers.
The WDT0 timer registers are accessed through port 65h and 22h (Address Index Register) and 23h (Data Register) ports. To access the registers, it is necessary to write the address of the port to port 22h, which data is read and/or written through the 23h port. Tables 2-7… 2-15 provide a detailed description of the WDT0 watchdog timer control registers.
The WDT1 timer registers are accessed through ports 67h - 6Dh. Tables 2-16 ... 2-22 below provide a detailed description of the WDT1 watchdog timer control registers.

Table 2-7 - WDT0 restart register

Address	Type of action	Bits							
		7	6	5	4	3	2	1	0
65h	Write	RST_WDT0							
	Read	-	-	-	-	-	-	-	-

Any writing to this port will lead to restart of the WDT0 timer.

Table 2-8 – Index register of the WDT0 port address

Address	Type of action	Bits							
		7	6	5	4	3	2	1	0
22h	Write	ADDR_REG_WDT0							
	Read	-	-	-	-	-	-	-	-

ADDR_REG_WDT0. Indicates the address of the selected WDT0 watchdog timer register for access via data register 23h.

Table 2-9 – Data register of the WDT0 port

Address	Type of action	Bits							
		7	6	5	4	3	2	1	0
23h	Write	WRDATA_REG_WDT0							
	Read	WRDATA_REG_WDT0							

WRDATA_REG_WDT0. Contains data for writing to the internal register of the WDT0 timer, which address is specified in the ADDR_REG_WDT0 field of the 22h index register.

WRDATA_REG_WDT0. Contains data when reading from the internal register of the WDT0 timer, which address is specified in the ADDR_REG_WDT0 field of the 22h index register.

Table 2-10 – Register of WDT0 timer control

Address (in the register of address 22h)	Action	Bits (in the data register 23h)							
		7	6	5	4	3	2	1	0
37h (40h)	Write	-	WDT0_WE	-	-	-	-	-	-
	Read	-	WDT0_WE	-	-	-	-	-	-

WDT1_WE. Permission for WDT1 watchdog timer operation.
1 – permitted (default value);
0 – prohibited.

Table 2-11 – Register of WDT0 event selection

Address (in the register of address 22h)	Action	Bits (in the data register 23h)							
		7	6	5	4	3	2	1	0
38h (D0h)	Write	WDT0_SSEL							
	Read								

WDT0_SSEL. Selecting an event at the end of the timer WDT0 counting.

0000 – reserved;
0001 – IRQ[3];
0010 – IRQ[4];
0011 – IRQ[5];
0100 – IRQ[6];
0101 – IRQ[7];
0110 – IRQ[9];
0111 – IRQ[10];
1000 – IRQ[11];

1001– IRQ[12];
1010– IRQ[14];
1011– IRQ[15];
1100 – NMI;
1101 – module reboot (default value);
1110 – reserved;
1111 – reserved.

Table 2-12 - Register CNT0 of the WDT0 timer value

Address (in the register of address 22h)	Action	Bits (in the data register 23h)							
		7	6	5	4	3	2	1	0
39h (00h)	Write	WDT0_CNT0							
	Read	WDT0_CNT0							

WDT0_CNT0. Bits [7:0] of the WDT_CNT[23:0] counter of WDT0 timer. Counter resolution is 30.5 µs.

Table 2-13 – Register CNT1 of the WDT0 timer value

Address (in the register of address 22h)	Action	Bits (in the data register 23h)							
		7	6	5	4	3	2	1	0
3Ah (00h)	Write	WDT0_CNT1							
	Read	WDT0_CNT1							

WDT0_CNT1. Bits [15:8] of the WDT0_CNT[23:0] counter of WDT0 timer. Counter resolution is 30.5 µs.

Table 2-14 - Register CNT2 of WDT0 timer value

Address (in the register of address 22h)	Action	Bits (in the data register 23h)							
		7	6	5	4	3	2	1	0
3Bh (20h)	Write	WDT0_CNT2							
	Read	WDT0_CNT2							

WDT0_CNT2. Bits [23:16] of the WDT0_CNT[23:0] counter of WDT0 timer. Counter resolution is 30.5 µs.

Table 2-15 –WDT0 timer state register

Address (in the register of address 22h)	Action	Bits (in the data register 23h)							
		7	6	5	4	3	2	1	0
3Ch (00h)	Write	WDT0_WDTF	WDT0_WDTRL	-	-	-	-	-	-
	Read	WDT0_WDTF	-	-	-	-	-	-	-

WDT0_WDTF. Flag of WDT0 timer triggering.

1 – timer was triggered (writing “1” to this bit resets the flag);

0 – timer was not triggered.

WDT0_WDTRL. WDT0 timer reboot.

1 – Reboot of the WDT0_CNT counter;

0 – This value is not allowed to be written.

Table 2-16 - WDT1 restart register

Address	Action	Bits							
		7	6	5	4	3	2	1	0
67h	Write	RST_WDT1							
	Read	-	-	-	-	-	-	-	-

Any writing to this port will force the WDT1 timer to restart.

Table 2-17 –WDT1 timer control register

Address	Action	Bits							
		7	6	5	4	3	2	1	0
68h (00h)	Write	-	WDT1_WE	-	-	-	-	-	-
	Read	-	WDT1_WE	-	-	-	-	-	-

WDT1_WE. Permission for WDT1 watchdog timer operation.

1 – Permitted;

0 – Prohibited (default value).

Table 2-18 - WDT1 event selection register

Address	Action	Bits							
		7	6	5	4	3	2	1	0
69h (00h)	Write	WDT1_SSEL				-	-	-	-
	Read	-	-	-	-	-	-	-	-

WDT1_SSEL. Selecting an even upon completion of the WDT1 timer counting.

0000 – Reserved (default value);

0001 – IRQ[3];

0010– IRQ[4];

0011– IRQ[5];

0100– IRQ[6];

0101– IRQ[7];

0110– IRQ[9];

0111– IRQ[10];

1000– IRQ[11];

1001– IRQ[12];

1010 – IRQ[14];
1011– IRQ[15];
1100 – NMI;
1101– module restart;
1110 – Reserved;
1111 – Reserved.

Table 2-19 – Register CNT0 of WDT1 timer value

Address	Action	Bits							
		7	6	5	4	3	2	1	0
6Ah (00h)	Write	WDT1_CNT0							
	Read	WDT1_CNT0							

WDT1_CNT0. Bits [7:0] of WDT1_CNT[23:0] counter of WDT1 timer. Counter resolution is 30.5 µs.

Table 2-20 – Register CNT1 of WDT1 timer value

Address	Action	Bits							
		7	6	5	4	3	2	1	0
6Bh (00h)	Write	WDT1_CNT1							
	Read	WDT1_CNT1							

WDT1_CNT1. Bits [15:8] of WDT1_CNT[23:0] counter of WDT1 timer. Counter resolution is 30.5 µs.

Table 2-21 – Register CNT2 of WDT1 timer value

Address	Action	Bits							
		7	6	5	4	3	2	1	0
6Ch (00h)	Write	WDT1_CNT2							
	Read	WDT1_CNT2							

WDT1_CNT2. Bits [23:16] of WDT1_CNT[23:0] counter of WDT1 timer. Counter resolution is 30.5 µs.

Table 2-22 - WDT1 timer state register

Address	Action	Bits							
		7	6	5	4	3	2	1	0
6Dh (00h)	Write	WDT1_WDTF	-	-	-	-	-	-	-
	Read	WDT1_WDTF	-	-	-	-	-	-	-

WDT1_WDTF. Flag of WDT1 timer triggering.
1 – timer was triggered (writing “1” to this bit resets the flag);
0 – timer was not triggered.

3 Installation and configuration

The device is made in PC/104-plus format. Expanding the functionality of the device is possible by connecting the additional PC/104 and PC/104-plus expansion modules.

3.1 Setting the switches

For hardware configuration of the device, the switches are used, which general description is given in Table 3-1.

Table 3-1 – Purpose of switches for device configuration

Switches	Description
SW1	Reset button
X1	Reset of BIOS Setup settings
X2	User switch. When setting the switch at input of the GPIO_P7[7] line, ‘0’ is read.
X3	Reset of the module when supplying the voltage ranging from 3 to 5.5 V to the XP18 connector’s pins.
X4, X5	COM3 port: connection of biasing resistor for 680 Ohm and 120 Ohm terminator to TX+/TX- lines
X6, X7	COM4 port: connection of biasing resistor for 680 Ohm and 120 Ohm terminators to TX+/TX- lines.

Description of the switches is given in the relevant sections of the paragraph “Structure and functioning”.

3.2 Configuring device parameters (BIOS SETUP)

The device configuration parameters are stored in the internal non-volatile ferromagnetic random-access memory (FRAM) and can be changed in BIOS Setup.

The device configuration parameters are set during booting, when the **<Del>** key is pressed on the keyboard connected to the USB port, by pressing **<F4>** key on the keyboard of the remote terminal, when the device is connected via the console serial COM-port.

4 Software

4.1 Basic software

Upon delivery, the integrated flash drive of the device contains programs that ensure the device's readiness for use: the built-in FreeDOS operating system.

The latest versions of the documentation, BIOS and utilities can be downloaded from the manufacturer's and distributor's ftp servers.

4.2 Establishing connection between PC and the device

To establish a connection between a personal computer (PC) and the device, you must:

1. When powered off, connect the VTC-9F cable with the null-modem adapter to the PC's COM port and the COM1 or COM2 connector of the device (by default, the COM1 port is set as the console port).
2. Install the terminal software suite supporting the data communications protocol XMODEM/CRC (e.g., HYPERTERMINAL, TELEMAX, TERM90, TERM95, PUTTY), with the parameters of serial line communication:
    1. PC port (COM1 / COM2)
    2. 8 bit data
    3. 1 stop bit
    4. No parity check
    5. Data exchange rate 115,200 bit/sec.
3. Turn on the power or press the RESET button if steps 1, 2 are not required and the power is on. If the connection is successfully established after booting the operating system, a DOS prompt line will appear on the PC screen: **C:>**
4. To boot the operating system without executing the commands of the **CONFIG.SYS** and **AUTOEXEC.BAT** files, after turning on the power or RESET, press the following key combination <Ctrl-B> or <Ctrl-C> for the step-by-step execution of commands.

4.3 Operation of the device with AT keyboard and VGA monitor

When connecting a USB keyboard and a VGA monitor to the device, the CPC314 controller can be used as a regular AT(x86)-compatible computer. Launching and debugging programs in this case is performed as usual and is not covered by this User Manual.

4.4 BIOS SOC Vortex86DX3 interface for reading serial number

To store the device parameters, the FRAM array is used. For storing the entire system information, the size of 1Kbyte is used (might slightly differ depending on BIOS version).

4.4.1 Array structure

```
_FRAM     STRUCT

          db        256 dup (0)        ; Reserve for storing the CMOS
copy

dSerNum dd          0                  ; Product serial number

_FRAM     ENDS
```

Service interrupt combined with printer service interrupt.

To call the service, the **INT 17H** interrupt is used with a parameter in the AH = 0ADh register.

The values of other parameters passed in processor registers are shown below.

Where the function number (AL) is specified incorrectly, AX = -1 (0FFFFh) is returned.

4.4.2 Obtaining serial number of the device

Input: AL = 6

Output: AX = result code (0 – no error)

CX:DX = serial number.

4.5 SOC Vortex86DX3 BIOS interface for reading/writing to FRAM

Integrated FRAM is also available for storing user data.

To call the FRAM read/write service, the **INT 17H** interrupt is used with a parameter in the AH = 0ADh register.

The values of other parameters transferred in processor registers are shown below. Where the function number (AL) is specified incorrectly, the AX = -1 (0FFFFh) is returned.

4.5.1 Reading user data from FRAM

Input: AL = 0Ch

BX = data start address in FRAM user area

CX = number of bytes read

DS:DX = indicates to the buffer for reading

Output:

AX = result code (0 – no error, -2 (0FFFEh) – parameter error, invalid address)

BX = maximum allowed address (size of the user area -1)

CX = number of bytes actually read

This function reads the specified bytes of the FRAM user area into the calling program's buffer.

4.5.2 Writing user data to FRAM

Input: AL = 0Dh

BX = data start address in FRAM user area

CX = number of bytes written

DS:DX = indicates to the written data

Output:

AX = result code (0 – no error, -2 (0FFFEh) – parameter error, invalid address)

BX = maximum allowed address (size of the user area -1)

CX = number of bytes actually written

* This function writes data to the FRAM user area.

4.6 Service programs

This chapter describes a set of drivers for working with I/O equipment connected to the device.

4.6.1 BIOS update utilities

The **ANYBIOS.EXE** program is designed for modifying the BIOS with writing to the integrated SPI-Flash of the processor in the device.

To modify BIOS, run the program with the "**w**" key and specify the BIOS file name "**bios.bin**" as a parameter and the key for skipping the MAC address recording of the Ethernet controller integrated into the processor:

anybios.exe w bios.bin skipmac

4.6.2 CMOS_RST.EXE utility (remote reset of BIOS settings)

The **CMOS_RST.EXE** is designed for resetting the BIOS settings to the default state (similar to the action of the BIOS Setup "Load Optimal Defaults" item). To reset the settings using the **CMOS_RST.EXE** program, you should connect the COM1 or COM2 port of the device of the product with a PC COM port with a null modem cable and turn on the power supply of the product (the settings will be reset and written to CMOS and FRAM, then a hardware reset will be

automatically carried out and the controller will start with the default settings). Windows OS must be installed on the PC you are using.

Syntax:

cmos_rst.exe [COM] where **[COM]** is the number of the COM-port used in the PC, this would be COM1 by default.

4.7 BIOS Update

The BIOS is stored in flash memory integrated into the Vortex86DX3 SoC and connected to the SPI interface.

During the BIOS update, please note that after the image update and reboot, the optimal (factory) BIOS Setup settings will be loaded. In this case, the console I/O settings will be changed to the factory settings (the Redirection After BIOS POST = "Boot Loader" mode). Therefore, if you need to use the integrated console I/O, then each time you boot the device during the BIOS update procedure, you must enter BIOS Setup and select the required settings for the console I/O and BIOS in general.

4.8 Switching the reference frequency for COM1, COM2, COM3, COM4

The default reference frequency for the Vortex86DX3 SoC integrated serial ports COM1, COM2, COM3, COM4 is set to 1.8432 MHz (24 MHz / 13). It is also possible to set the reference frequency of 24 MHz and 48 MHz.
Setting the reference clock frequency for COM1..4 is available through the registers in PCI Config Space Bus: Dev: Func - 00.07.00 (0x00003800)

UART1 - Reg 0x50 bit 30 (UART clock selection. 0: 24MHz/13 (default), 1: 24MHz)
UART2 - Reg 0xA0 bit 22 (UART clock selection. 0: 24MHz/13 (default), 1: 24MHz)
UART3 - Reg 0xA4 bit 22 (UART clock selection. 0: 24MHz/13 (default), 1: 24MHz)
UART4 - Reg 0xA8 bit 22 (UART clock selection. 0: 24MHz/13 (default), 1: 24MHz)

Switching example (DOS, WatcomC or BorlandC):

```
#include <conio.h>
#include <dos.h>
void Set_Base24MHz_UART1()
{
        uint32_t pci_reg;
        disable();                          // disable interrupts
        outpd( 0xCF8, 0x80003850 );         // pci_cfg_index
        pci_reg = inpd( 0xCFC );            // read
        pci_reg = pci_reg | 0x40000000;     // set BIT30 (UART1)
       // pci_reg = pci_reg | 0x00400000;   // set BIT22 (UART2..4)
        outpd( 0xCF8, 0x80003850 );         // pci_cfg_index
```

```
        outpd( 0xCFC, pci_reg );            // write register
        enable();                           // enable interrupts
}
```

If the “SB Clock” parameter in BIOS Setup is set to “100 MHz” (Advanced → South Bridge Configuration → ISA Configuration), then this function will set the reference frequency not to 24 MHz, but to 48 MHz. When the “SB Clock” parameter is set in BIOS Setup by default (100 MHz), the Set_Base24MHz_UART1 () function will set the reference frequency to 48 MHz.

Attention!

Changing the value of the “SB Clock" parameter influences over the frequency of ISA bus.

4.9 Working with I2C devices

As an example of working with i2c devices, you can use the vortex86_i2c library (library files “vortex86_i2c.c”, “vortex86_i2c.h” and sample files are available on the manufacturer's and distributor's ftp servers.

The library is collected within a free Open Watcom C/C ++ package.

The library implements the following functions:

- uint16_t **I2C_GetBase**() – returns the base address in the I/O space used for i2c buses
- void **I2C_SetBase**(uint16_t ba) – sets a base address in the I/O space that is used for i2c buses
- void **I2C_PowerOff**(uint8_t channel) – disables the specified i2c bus
- void **I2C_PowerOn**(uint8_t channel) – enables the specified i2c bus
- uint16_t **I2C_Init**(uint8_t channel) – configures the specified bus and returns the base address
- uint16_t **I2C_Start**(uint8_t channel, uint8_t addr, uint8_t gen_stop, uint16_t timeout) – generates the start on the bus and sets the device address. The function will return the remainder of the timeout parameter
- uint16_t **I2C_ReadByte**(uint8_t channel, uint8_t * dat, uint8_t lastbyte, uint16_t timeout) – reads one byte. For the last byte, the lastbyte parameter must not be equal to 0. The function returns the remainder of the timeout parameter
- uint16_t **I2C_WriteByte**(uint8_t channel, uint8_t dat, uint8_t lastbyte, uint16_t timeout) – writes one byte. For the last byte, the lastbyte parameter must not be equal to 0. The function returns the remainder of the timeout parameter
- uint16_t **I2C_ReadByteReg**(uint8_t channel, uint8_t addr, uint8_t reg, uint8_t * dat, uint16_t timeout) reads a byte from the i2c device with the addr address from register reg. The function will return the remainder of the timeout parameter
- uint16_t **I2C_ReadWordReg**(uint8_t channel, uint8_t addr, uint8_t reg, uint16_t * dat, uint16_t timeout) reads a word from i2c device with the addr address from register reg. The function will return the remainder of the timeout parameter
- uint16_t **I2C_WriteByteReg**(uint8_t channel, uint8_t addr, uint8_t reg, uint8_t dat, uint16_t timeout) writes a byte to the i2c device with the addr address to register reg. The function will return the remainder of the timeout parameter
- uint16_t **I2C_WriteWordReg**(uint8_t channel, uint8_t addr, uint8_t reg, uint16_t dat, uint16_t timeout) writes a word to i2c device with the addr address to register reg. The function will return the remainder of the timeout parameter

Example of working with the TMP75 digital temperature sensor (Texas Instruments)

Address of the TMP75 chip is set on the I2C bus

```
#define TMP75_WR_ADDR          0x90
```

First, the bus is configured

```
I2C_SetBase( I2C_DEF_BASE_ADDR );

I2C_Init( I2C_CHANNEL0 );
```

Next, the chip's identifier is read

```
timeout = I2C_ReadWordReg( I2C_CHANNEL0, TMP75_WR_ADDR, 0x07, &id, DEF_TIMEOUT );
```

If the identifier is correct, the temperature will be read

```
timeout = I2C_ReadWordReg( I2C_CHANNEL0, TMP75_WR_ADDR, 0x00, &rd_temp, DEF_TIMEOUT
);
```

Converted to the usual form and routed to the console

```
temp = 1;
rd_temp = rd_temp >> 3;
if( rd_temp & 0x2000 ) {
temp = -1; rd_temp = 0x2000 - rd_temp;
}
temp = temp * rd_temp * 0.0625;
printf( " Temperature=%.4f\r\n", temp );
```

5 Basic Input / Output System (BIOS)

To enter BIOS Setup, while booting the system during the POST (Power On Self Test) procedure, press the DEL key on the keyboard or the F4 key on the console PC keyboard (when the Console Redirect option is enabled). An example of the screen during the POST procedure is shown in Fig. 5-1.

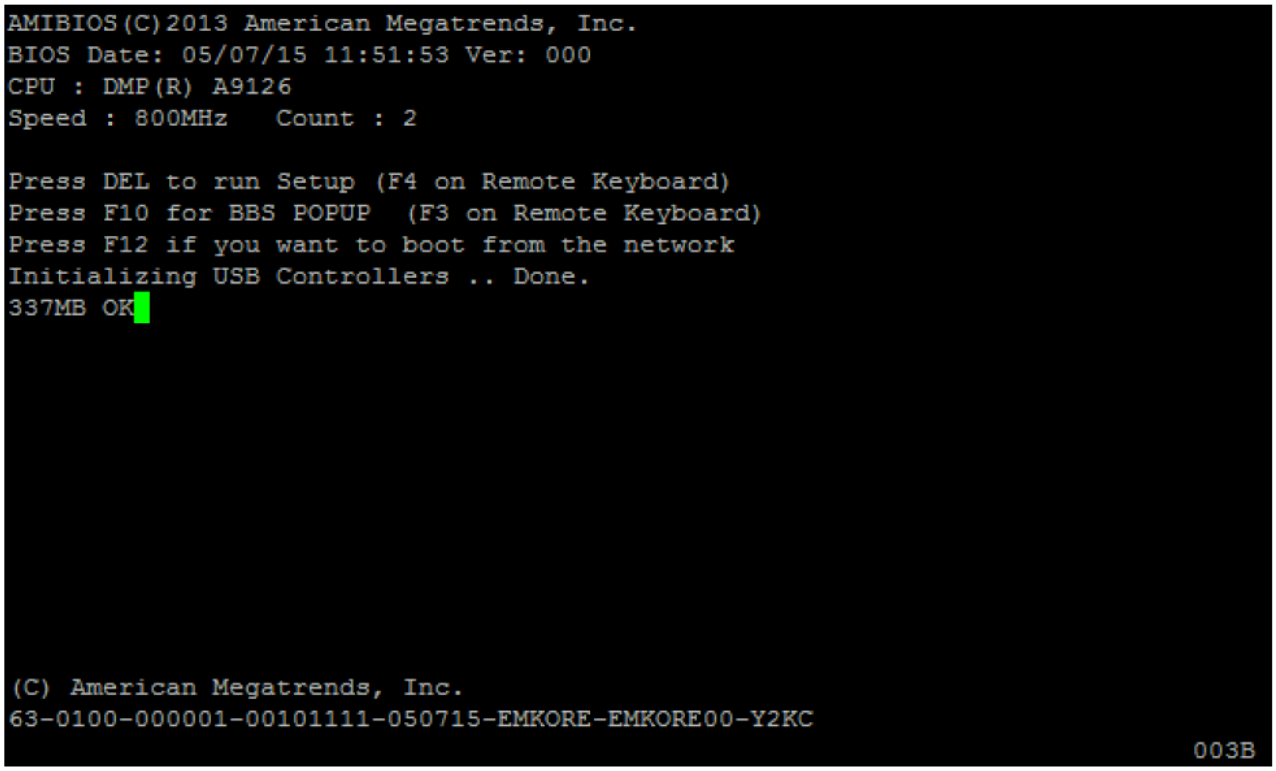


Fig. 5-1 – Screen during the device boot (POST)

Using the BIOS Setup Utility, you can change the BIOS (Basic Input Output System) parameters and control special modes of the device. This program uses the menu system to make changes and to enable or disable special features.

The information fields (highlighted in gray) are used to display additional information on the device and/or its settings and are not available for changes by the user. Default values are underlined when describing menu items. Information fields are italicized. Setting incorrect values can lead to system malfunctions.

Attention!

To reset BIOS Setup settings where it is impossible to enter the settings menu, you must use the cmos_rst.exe utility for remote reset via the COM port (COM1, COM2).

5.1 Main

This tab contains description of BIOS version, RAM and CPU installed. There are also two items responsible for setting the current time and date. The Main menu screen and item descriptions are shown below.

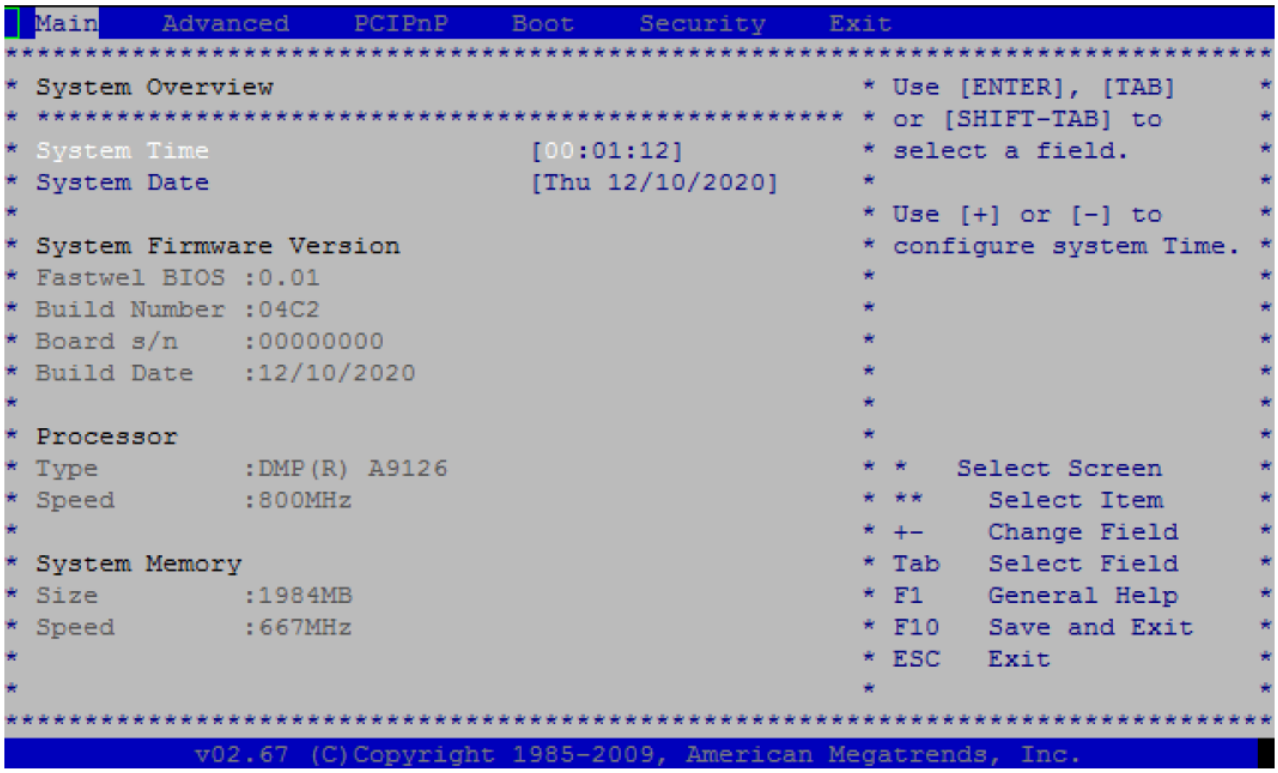


Fig. 5-2 – Screen of the "Main" menu

Table 5-1 – Description of the "Main" menu

Menu item	Purpose
System Firmware Version *(BIOS version information)*	*Fastwel BIOS (current BIOS version)* *Build Number* *Board s/n* *Build Date*
Processor *(Information field)*	Information related to the CPU installed: *DMP(R) Vortex A9126* – version of the Vortex86DX3 processor *Speed* – processor clock speed
System Memory *(Information field)*	Information on the DDR2 SDRAM installed: *Size* *Speed*
System Time	Current time in the format [hour/min/sec]
System Date	Current date in the format [month/date/year]

5.2 Advanced

This tab contains the items responsible for the operation of the soldered ATA Flash Disk, processor Cache memory, IDE bus, console I/O and USB devices. The “Advanced” menu screen and item descriptions are shown below.

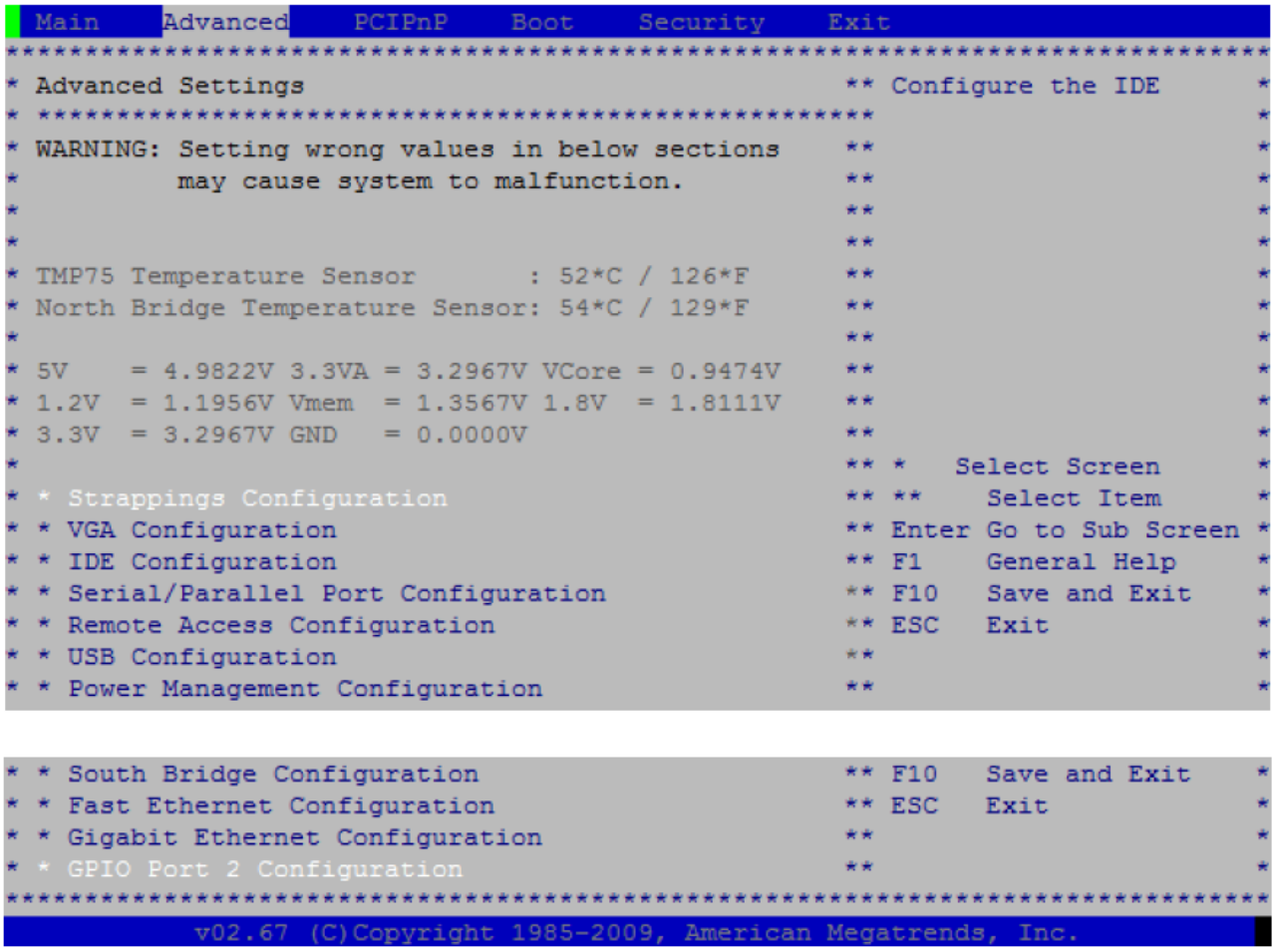


Fig. 5-3 – Screen of the “Advanced” menu

Table 5-2 – Description of the “Advanced” menu

Menu item	Purpose
Strapping Configuration (submenu)	Configuring system operation parameters (processor frequency, memory, internal bus, number of active processor cores) * the menu appears when you activate the “RDC Engineer Mode” on the "Security" BIOS Setup page
VGA Configuration (submenu)	Integrated video controller settings
IDE Configuration (submenu)	Controlling operation of the devices on IDE / SATA / SD bus
Serial / Parallel Port Configuration (submenu)	Settings of the serial and parallel ports
Remote Access Configuration (submenu)	Console I/O settings
Menu item	**Purpose**

USB Configuration (submenu)	Settings of USB ports. These settings apply to all 4 USB ports
Power Management Configuration (submenu)	ACPI, APM settings
Smbios Configuration (submenu)	SMBIOS settings
South Bridge Configuration (submenu)	South Bridge settings

5.2.1 IDE Configuration

Screen of the “IDE Configuration” menu and description of items are given below.

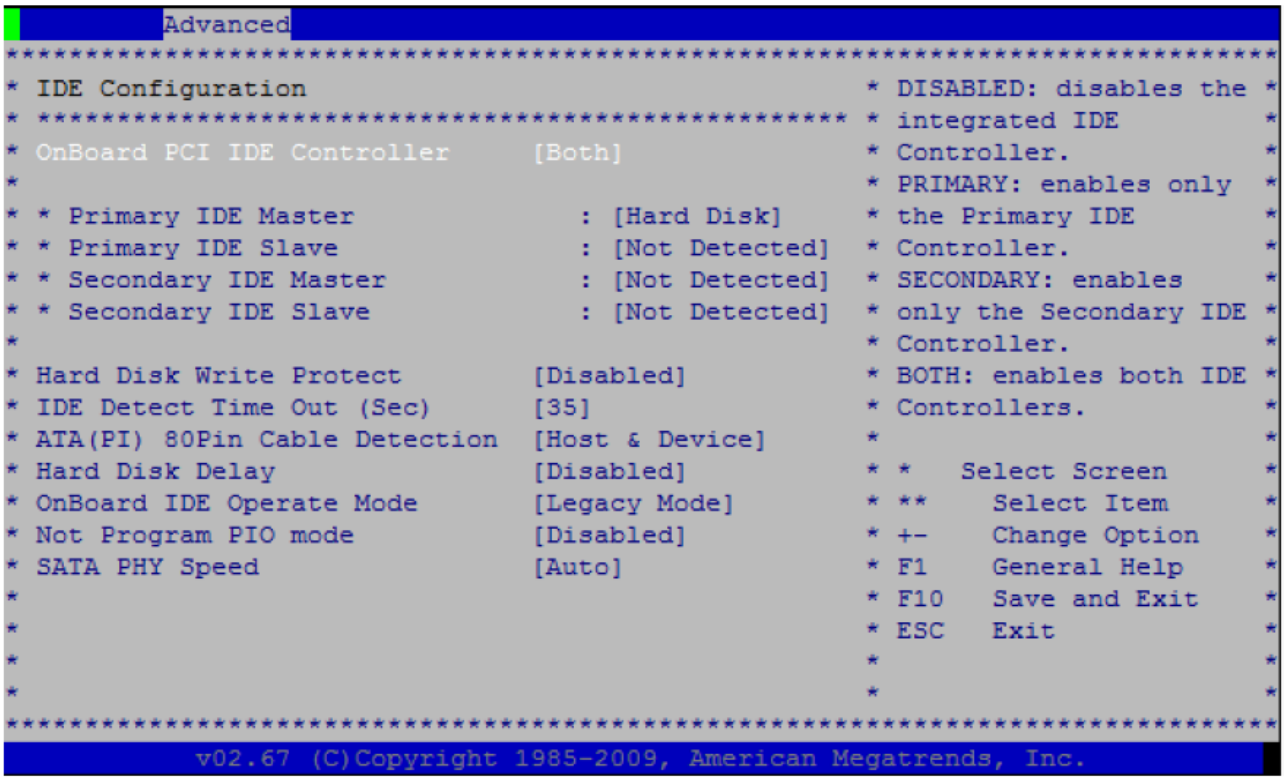


Fig. 5-4 – Screen of the “IDE Configuration” menu

Table 5-3 – Description of the “IDE Configuration” menu

Menu item	Purpose	
Onboard PCI IDE Controller	Control of operation of integrated PCI controller of IDE bus.	
	[Both][9]	Operation is enabled
	[Disabled]	Operation is disabled
Primary IDE Master (submenu)	This item provides information about the connected IDE device operating in Master mode if a card is installed in microSD slot.	

[9] Here and below, underlining means that the parameter value is selected by default.

Menu item	Purpose	
Primary IDE Slave (submenu)	Not used.	
Secondary IDE Master (submenu)	This section stores information on the connected IDE device, working in the Master mode. External SATA drive.	
Secondary IDE Slave (submenu)	Not used.	
Hard Disk Write Protect	Permission for setting the protect for writing to IDE devices	
	[Enabled]	Enable the protect
	[Disabled]	Disable the protect
IDE Detect Time Out (Sec)	Waiting limit for determining ATA/ATAPI device, in seconds. Available values are:	
	[0], [5], [10], [15], [20], [25], [30] ,[35]	
ATA(PI) 80Pin Cable Detection	Selecting a method for identifying an 80-core ATA(PI) cable	
	[Host & Device]	Check by system and IDE devices
	[Host]	Check by the system only
	[Device]	Check by the IDE device only
Hard Disk Delay	Additional delay when identifying IDE devices	
	[Disabled]	Delay is disabled
	[1], [2], [4], [8]	Time for additional delay in seconds
Onboard IDE Operate Mode	IDE controller operation mode	
	[Legacy]	Legacy mode is selected
	[Native]	Native mode is selected (only for Windows XP and 7)
SATA PHY Speed	Selection of the SATA PHY operation mode	
	[Auto]	Automatic selection of the SATA operation mode
	[Gen1 Only]	Limitation of the SATA operation mode (Gen1 only)

5.2.1.1 Primary IDE Master

The screen of the “Primary IDE Master” and description of the items are given below. The “IDE Primary Master and Slave” menus are fully identical to the “Secondary IDE Master” menu.

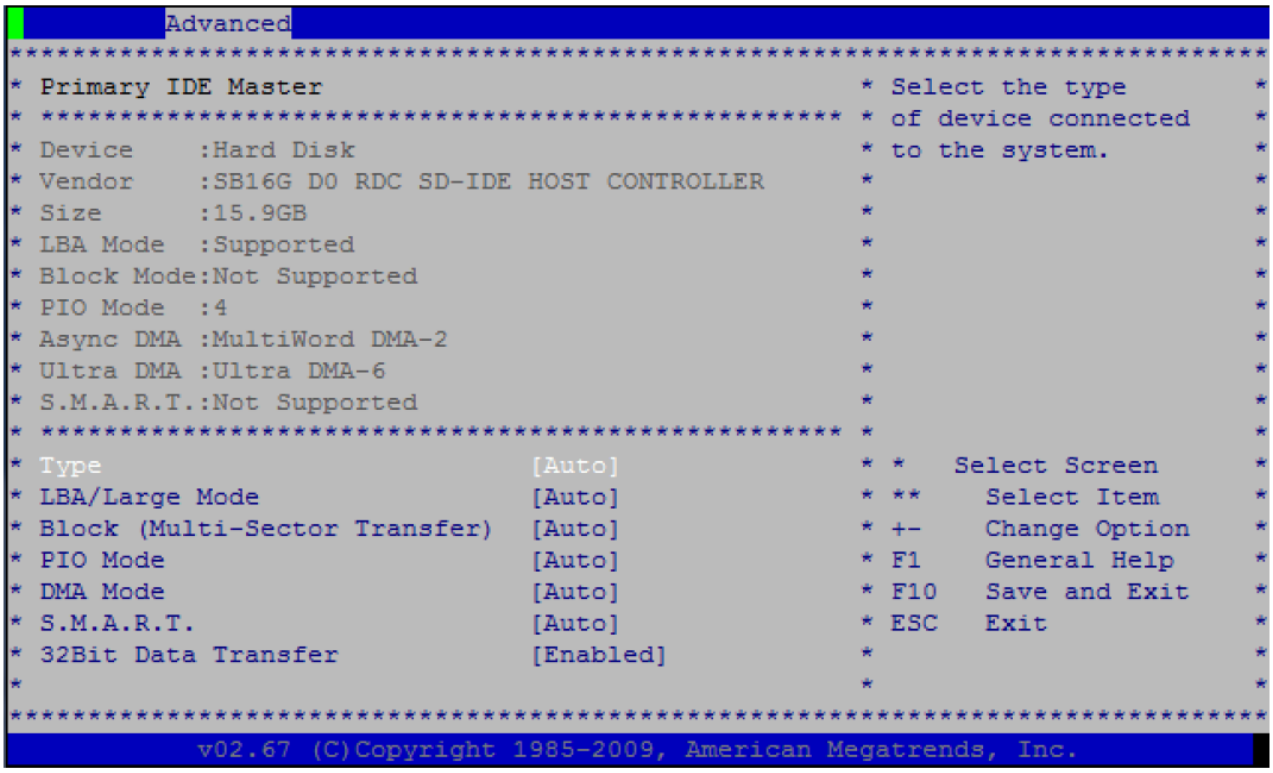


Fig. 5-5 – Screen of the “Secondary IDE Master” menu

Table 5-4 – Description of the “Primary IDE Master” menu

Menu item	Purpose	
Type	Type of the device, connected to this IDE channel	
	[Not Installed]	Prohibition against the search for connected devices
	[Auto]	Automatic detection of the connected device type
	[CD/DVD]	Identify the connected device as the CD/DVD drive
	[ARMD]	Identify the connected device as the ATAPI removable media (ZIP, LS-120)
LBA/Large Mode	Addressing type of the device connected to this IDE channel	
	[Auto]	Automatic detection of LBA mode support
	[Disabled]	Prohibition against LBA mode detection, the Large Mode is used
Block (Multi-Sector Transfer)	Block data transfer mode	
	[Auto]	This option allows the BIOS to automatically detect whether the Multi-Sector Transfers mode is supported on the current channel. This option allows the BIOS to automatically detect the amount of sectors per block for transfer from hard drive to memory. Data to/from the device will be transmitted several sectors per unit of time. The default value.

Menu item	Purpose	
	[Disabled]	This option disables BIOS from using the Multi-Sector Transfer mode on the current channel. Data to/from the device will be transmitted one sector per unit of time.
PIO Mode	Programmed I/O (PIO) mode	
	[Auto]	This option allows BIOS to automatically determine if the device supports the PIO mode. This setting is recommended to be used when it is impossible to determine the supported mode of the connected device.
	[0]	Set the PIO 0 mode for the connected device. The data transfer rate in this mode is up to 3.3 MB/sec.
	[1]	Set the PIO 1 mode for the connected device. The data transfer rate in this mode is up to 5.2 MB/sec.
	[2]	Set the PIO 2 mode for the connected device. The data transfer rate in this mode is up to 8.3 MB/sec.
	[3]	Set the PIO 3 mode for the connected device. . The data transfer rate in this mode is up to 11,1. MB/sec.
	[4]	Set the PIO 4 mode for the connected device. The data transfer rate in this mode is up to 16.6. MB/sec.
DMA Mode	DMA (Direct Memory Access) data transfer mode	
	[Auto]	Recommended value for the most efficient data transfer. BIOS will automatically detect the most suitable DMA mode.
	[SWDMA0] [SWDMA1] [SWDMA2]	“Single Word DMA” modes
	[MWDMA0] [MWDMA1] [MWDMA2]	“Multi Word DMA” modes
S.M.A.R.T.	Smart Monitoring, Analysis, and Reporting Technology	
	[Auto]	BIOS will automatically detect and support the connected device. It is recommended to use this option if detection and support of the connected drive is impossible.
	[Enabled]	This option enables BIOS to use the SMART function when working with the connected drives
	[Disabled]	This option disables BIOS from the use of SMART function when working with the connected drives.
32-bit Data Transfer	32-bit data transfer mode	
	[Enabled]	This option enables the use of 32-bit data transfer for the connected device.
	[Disabled]	This option disables the use of 32-bit data transfer for the connected device.

5.2.2 Remote Access Configuration

Screen of the “Remote Access Configuration” menu and description of the items are given below.

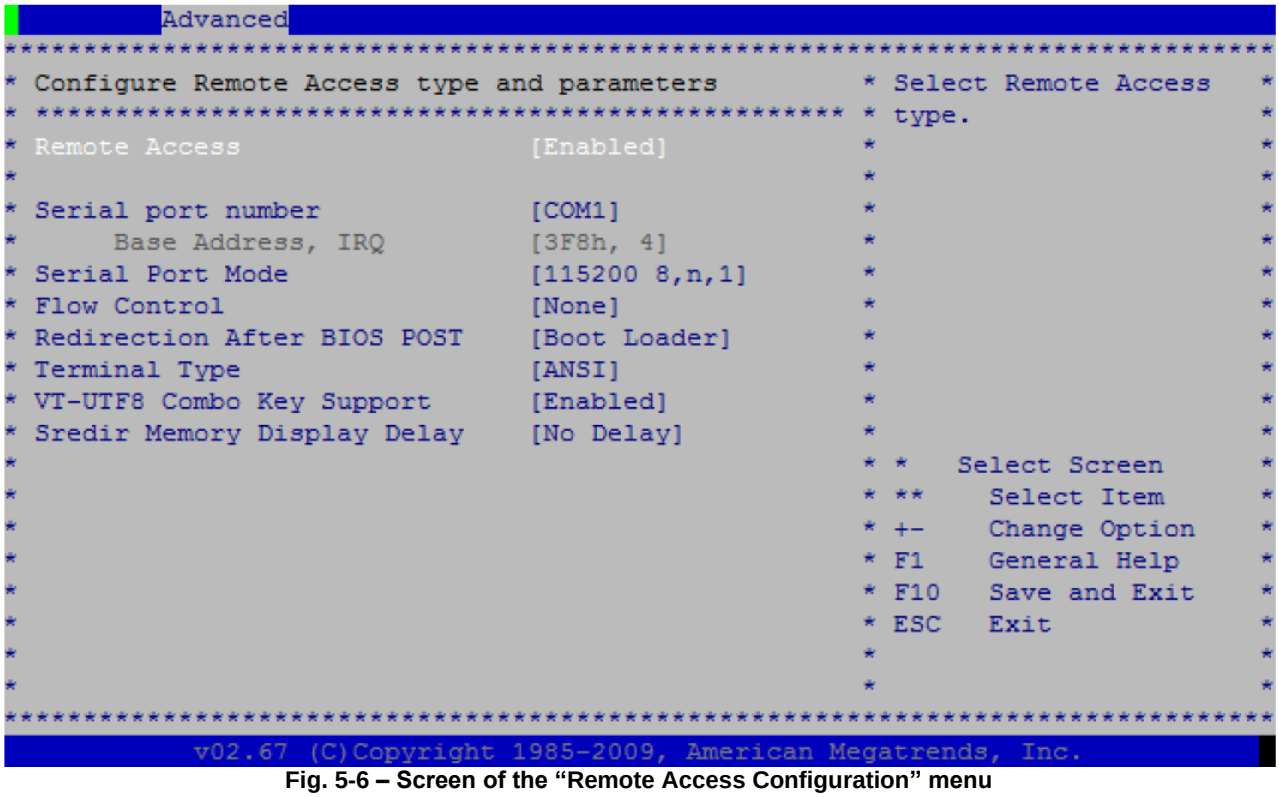


Fig. 5-6 – Screen of the “Remote Access Configuration” menu

Table 5-5 – Description of the “Remote Access Configuration” menu

Menu item	Purpose	
Remote Access	Console I/O	
	[Disabled]	Console I/O is disabled
	[Enabled]	Console I/O is enabled, additional options for configuring console I/O parameters become available.
Serial port number	Selecting the console I/O serial port	
	[COM1]	COM1 port is used as a console I/O port
	[COM2]	COM2 is used as a console I/O port
	[COM3]	COM3 is used as a console I/O port
	[COM4]	COM4 port is used as a console I/O port
Serial port mode	Operation mode of the console I/O port	
	[115200 8,n,1],	Data transfer rate 115.2 kbaud, 8-bit, no parity check, 1 stop bit
	[57600 8,n,1],	Data transfer rate 57.6 kbaud, 8-bit, no parity check, 1 stop bit
Menu item	**Purpose**	
	[38400 8,n,1],	Data transfer rate 38.4 kbaud, 8-bit, no parity check, 1 stop bit
	[19200 8,n,1],	Data transfer rate 19.2 kbaud, 8-bit, no parity check, 1 stop bit
	[09600 8,n,1],	Data transfer rate 9.6 kbaud, 8-bit, no parity check, 1 stop bit
Flow Control	Controlling the stream of characters for console port	

	[None]	No
	[Hardware]	CTS/RTS hardware control
	[Software]	XON/XOFF software control
Redirection After BIOS POST	The mode of the console I/O port operation after passing the POST procedure by the BIOS	
	[Disabled]	Disabling the console I/O after passing POST by BIOS
	[Boot Loader]	Console I/O is active during the time BIOS passes the POST procedure and at the time of OS system booting
	[Always]	Console I/O is always active. Some operating systems may not work while this option is selected.
Terminal Type	Type of the terminal	
	[ANSI]	ANSI standard
	[VT100]	VT100 standard
	[VT-UTF8]	VT-UTF8 standard
VT-UTF8 Combo Key Support	Support of VT-UTF8 symbols for ANSI/ME100 terminals	
	[Disabled]	Support is disabled
	[Enabled]	Support is enabled
Sredir Memory Display Delay	Delay with device loading when displaying information about installed RAM to console PC	
	[No Delay]	No delay
	[Delay 1 Sec],	Set the delay of 1 sec.
	[Delay 2 Sec],	Set the delay of 2 sec.
	[Delay 4 Sec]	Set the delay of 4 sec.

5.2.3 USB Configuration

Screen of the “USB Configuration” menu and description of items is given below.

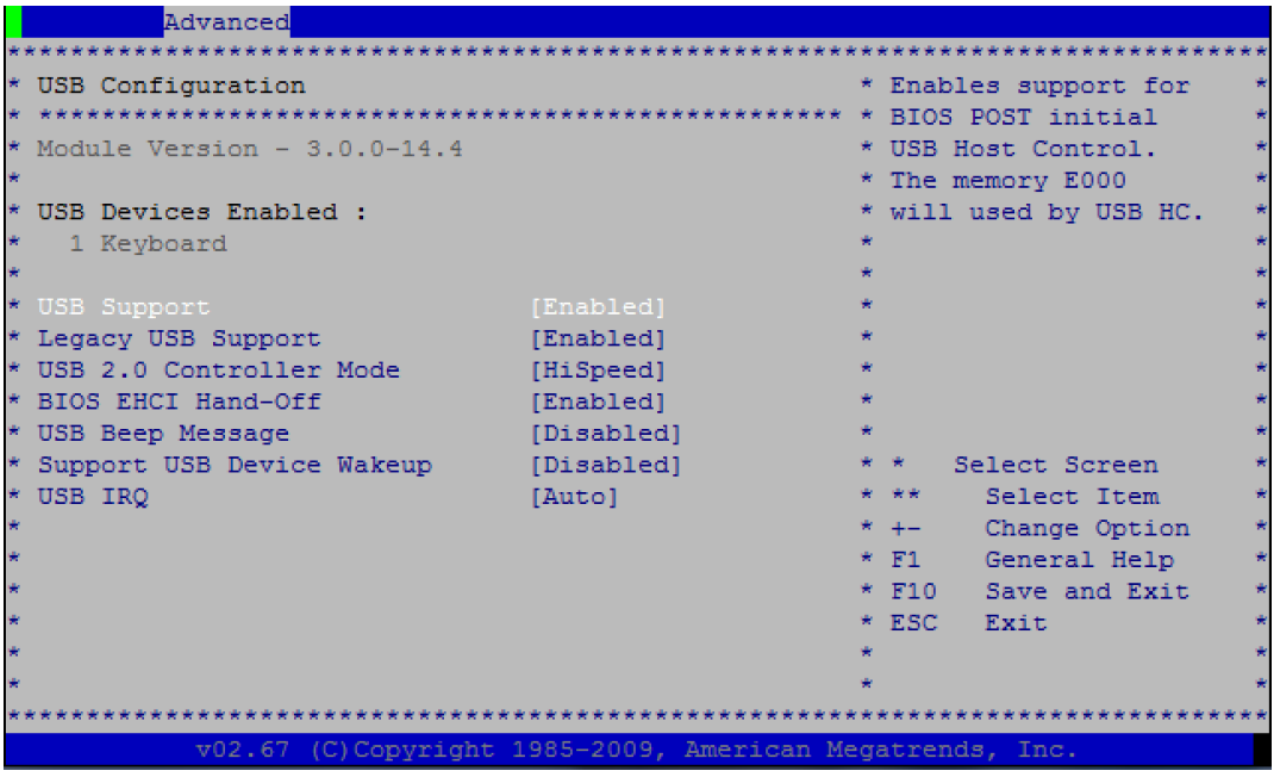


Fig. 5-7 – Screen of the “USB Configuration” menu

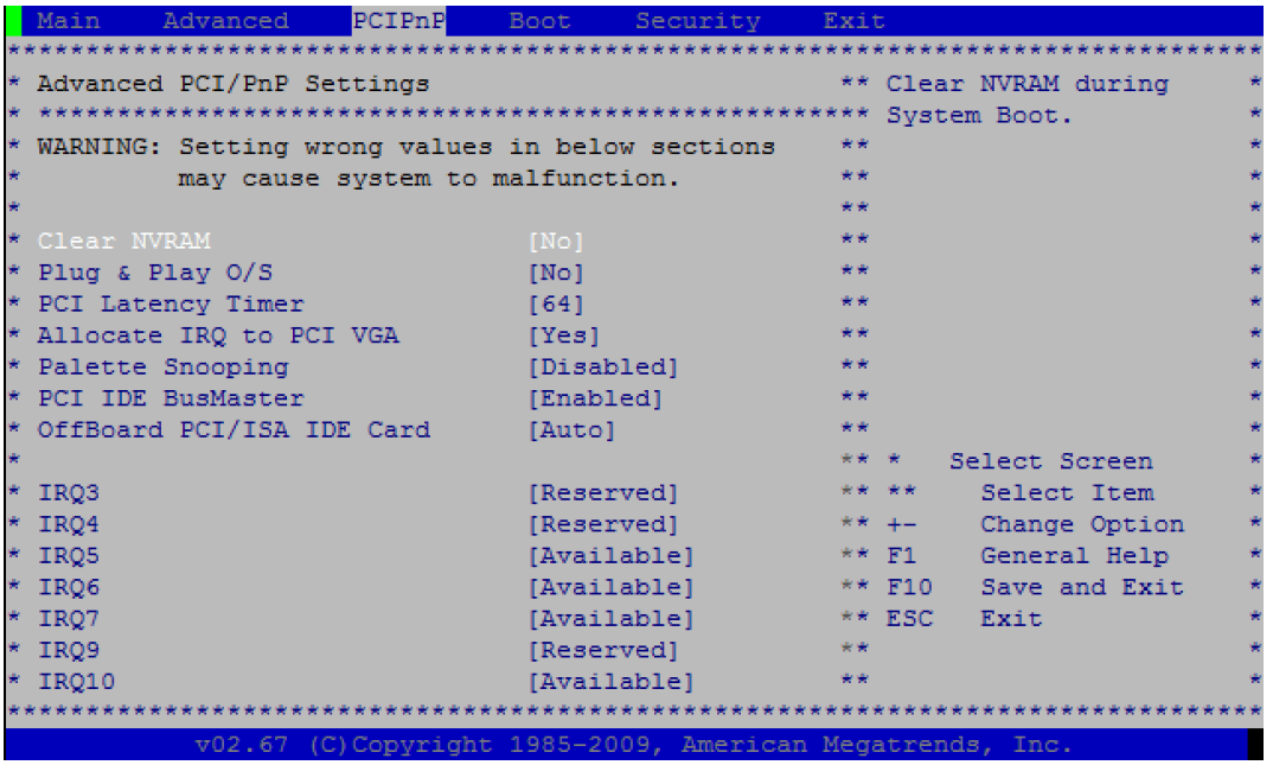
Table 5-6 – Description of the “USB Configuration” menu

Menu item	Purpose	
USB Support	Support of USB Host during BIOS Post.	
	[Disabled]	USB Host Control mode is disabled
	[Enabled]	USB Host Control mode is enabled
Legacy USB Support	Support of Legacy USB mode.	
	[Disabled]	Legacy USB mode is disabled
	[Enabled]	Legacy USB mode is enabled
	[Auto]	Activation of the Legacy USB mode only if at least one USB device is connected
USB 2.0 Controller Mode	Determining the data exchange rate with a USB device	
	[HiSpeed]	Data exchange rate 25-480 Mb/s
	[FullSpeed]	Data exchange rate 0.5-12 Mb/s (mode USB 1.0/1.1)
BIOS EHCI Hand-Off	BIOS support for the mechanism of control transfer between devices Enhanced Host Controller Interface (EHCI)	
	[Disabled]	Controlled by operating system
	[Enabled]	Controlled by BIOS
USB Beep Message	Beeping when connected USB devices are detected	

	[Disabled]	Controlled by operating system
Menu item	**Purpose**	
	[Enabled]	Controlled by BIOS
Support USB Device Wakeup	Enabling support for USB device wakeup	
	[Disabled]	Support is disabled
	[Enabled]	Support is enabled
USB IRQ	Configuring the interrupt line used by the USB controller	
	[Auto]	Automatic selection
	[use IRQ 5]	IRQ5 is used
	[use IRQ 6]	IRQ6 is used

5.3 PCI / PnP

This tab contains items responsible for the operation of PCI and ISA buses, as well as interrupt switching management. The screen of PCI/PnP menu and menu descriptions are shown below.



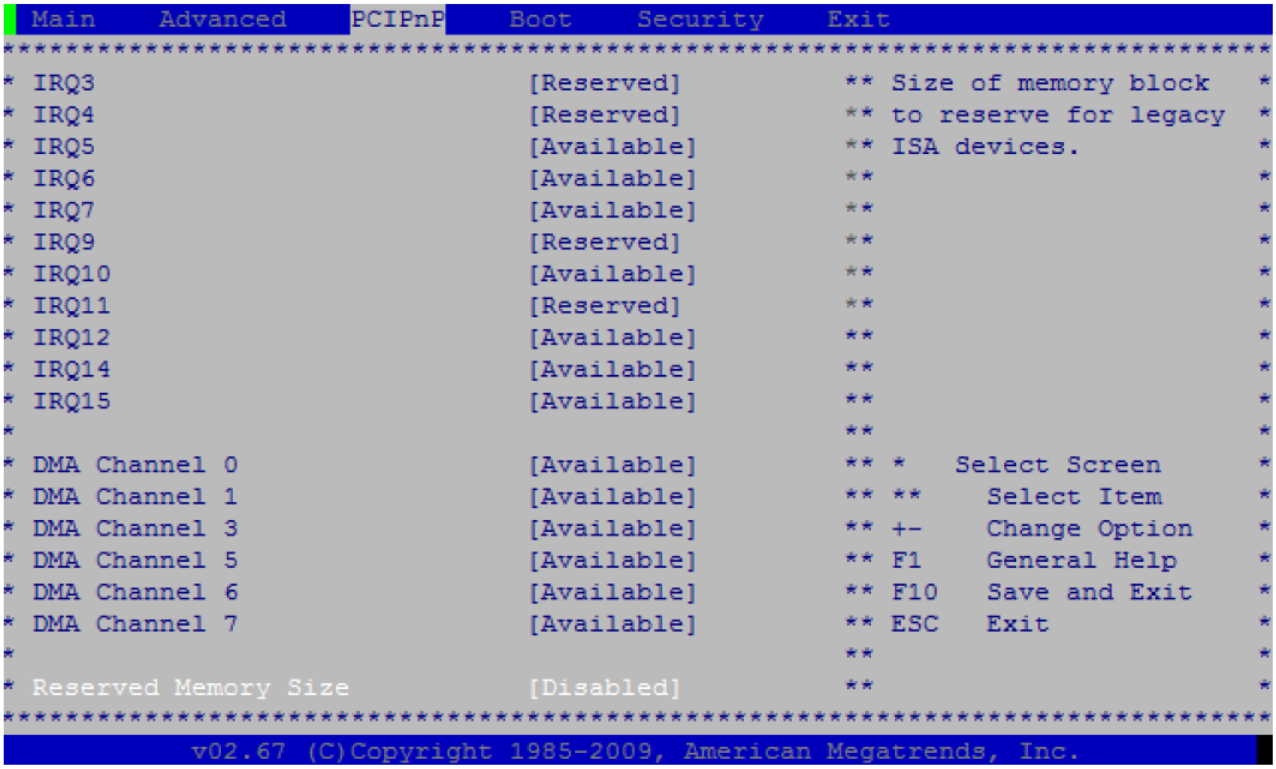


Fig. 5-8 – Screen of the "PCI/ PnP" menu

Table 5-7 – Description of the "PCI/ PnP" menu

Menu item	Purpose	
Clear NVRAM	Reset of PnP parameters table	
	[No]	Without change
	[Yes]	Reset the table after reboot
Plug & Play O/S	OS with PnP support is installed	
	[No]	No
	[Yes]	Yes
PCI Latency Timer	The maximum number of PCI bus cycles during which a device connected to this bus can keep it busy while transferring the data.	
	[32], [64], [96], [128], [160], [192], [224], [248]	
Allocate IRQ to PCI VGA	Allowing the interrupt assignment to the graphics card on the PCI bus	
	[No]	Do not assign the PCI interrupt to the graphics card
	[Yes]	Assign the PCI interrupt to the graphics card
Palette Snooping	Synchronizing the colors of the graphics card and the image captured using the I/O graphics card (video editing card).	
	[Disabled]	The function is disabled. Recommended value
	[Enabled]	The function is enabled
PCI IDE BusMaster	Enabling the Bus Mustering PCI Mode for the IDE Bus Controller	

	[Disabled]	Disable the use of the Bus Mastering Mode
	[Enabled]	Enable the use of the Bus Mastering Mode
OffBoard PCI/ISA IDE Card	Selecting an external PCI/ISA card for the IDE bus controller	
	[Auto]	Automatic detection of the presence of PCI/ISA card of the IDE bus controller. Recommended value.
	[PCI Slot1], [PCI Slot2], [PCI Slot3], [PCI Slot4], [PCI Slot5], [PCI Slot6]	Indicate that an IDE bus controller card is installed in the relevant PCI slot
IRQ3 IRQ4 IRQ5 IRQ6 IRQ7 IRQ9 IRQ10 IRQ11 IRQ12 IRQ14 IRQ15	Reservation of IRQ interrupt for internal Legacy devices Vortex86DX3	
	[Available]	Enable the use of this interrupt by the PCI/PnP devices
	[Reserved]	Disable the use of this interrupt by the PCI/PnP devices, reserve for the Legacy devices. Setting to the “Reserved” option will enable to use the IRQ line by external ISA devices (not PnP). To use the IRQ line by external ISA devices (not PnP) you need to make sure that the line is unoccupied by other internal Vortex86DX3 devices.
DMA Channel 0 DMA Channel 1 DMA Channel 3 DMA Channel 5 DMA Channel 6 DMA Channel 7	Reservation of DMA channel for internal Legacy Vortex86DX3 devices	
	[Available]	Enable the use of this DMA channel by the PCI/PnP devices
	[Reserved]	Disable the use of this DMA channel by the PCI/PnP devices, reserve for the Legacy devices.
Reserved Memory Size	Reserving memory for ISA bus devices by BIOS program	
	[Disabled]	Disable reserving memory for ISA bus devices by BIOS. Recommended value.
	[16k], [32k], [64k]	Reserve the specified memory capacity for ISA bus devices

5.4 Boot

This tab contains menu items responsible for device booting modes, as well as for choosing an IDE device which will be used for booting the operating system. The screen of the “Boot” menu and description of menu items are specified below.

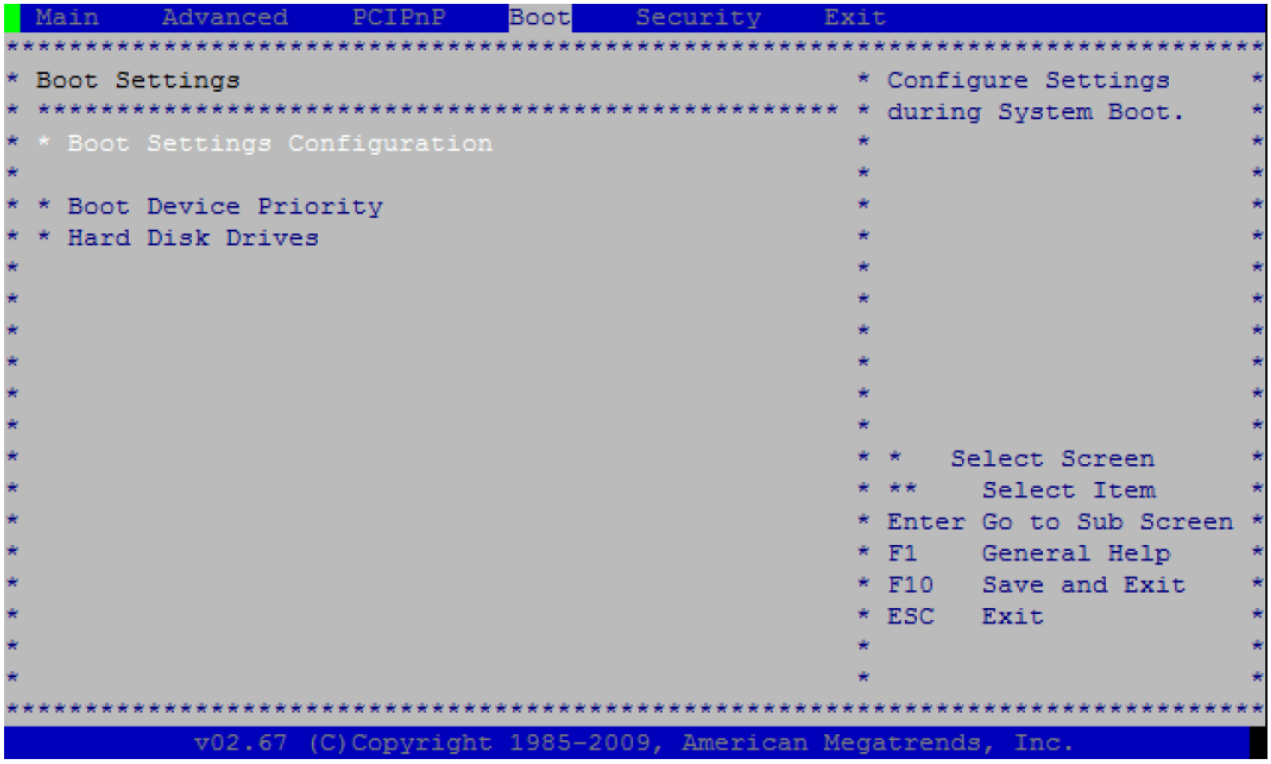


Fig. 5-9 – Screen of the “Boot” menu

Table 5-8 – Description of the “Boot” menu

Menu item	Purpose
Boot Settings Configuration (submenu)	Boot settings configuration
1st Boot Device Priority (submenu)	Priority of boot devices
Hard Disk Drives (submenu)	Connected drives

5.4.1 Boot Settings Configuration

Screen of the “Boot Settings Configuration” menu and description of the menu items are given below.

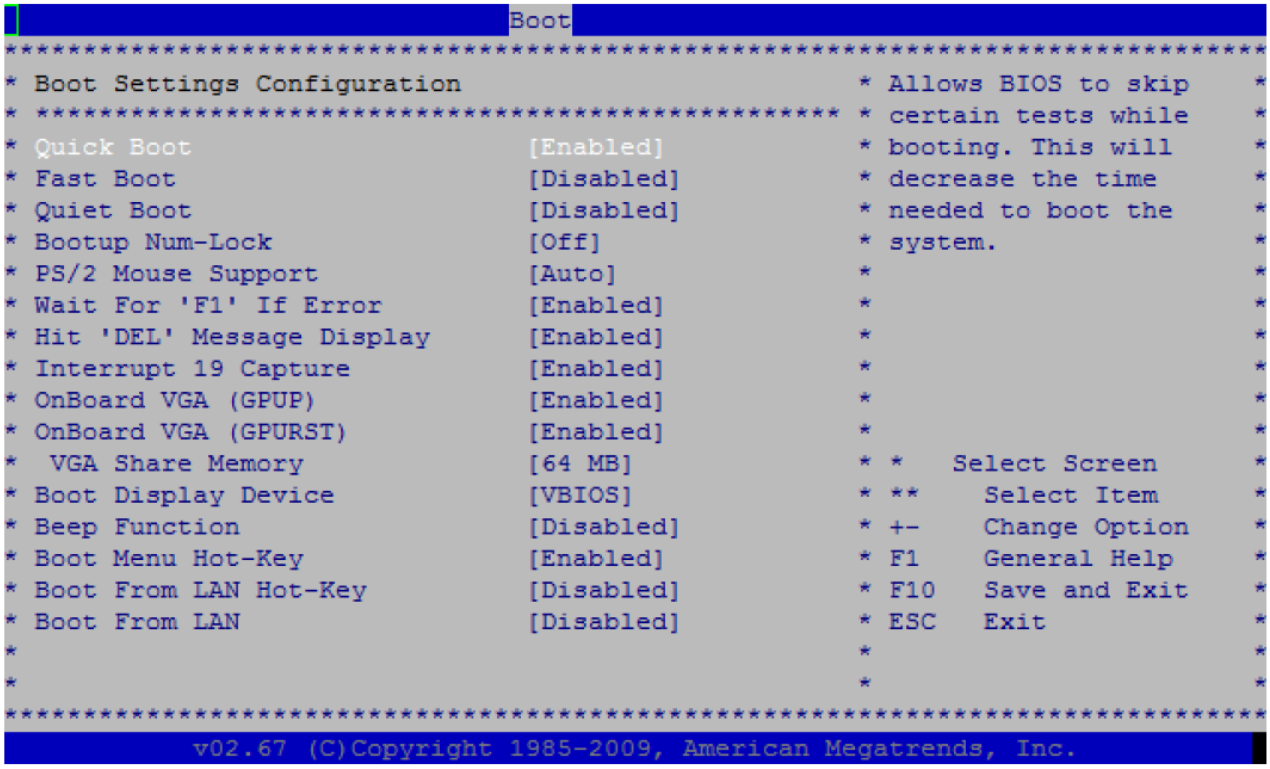


Fig. 5-10 – Screen of the “Boot Settings Configuration” menu

Table 5-9 – Description of the “Boot Settings Configuration” menu

Menu item	Purpose	
Quick Boot	Quick boot	
	[Disabled]	Choosing this value provides a complete self-test of the system when the power is switched on.
	[Enabled]	Choosing this value allows you to reduce the number of tests at the time of power-on and by doing so speed up the boot process.
Add On ROM Display Mode	The mode for displaying expansion cards	
	[Force BIOS]	This value allows displaying data from the BIOS of expansion cards to the monitor at the time of system boot.
	[Keep Current]	This value allows the computer system to display only P.O.S.T. information during the boot time
Bootup Num-Lock	Num Lock during the boot process	
	[Off]	Disabling the Num Lock during the boot process
	[On]	Enabling Num Lock during the boot process
PS/2 Mouse Support	Support of PS/2 mouse	
	[Disabled]	Support is disabled

	[Enabled]	Support is enabled
Menu item	**Purpose**	
	[Auto]	Automatic detection of support. Recommended value
Wait for 'F1' If Error	Waiting for F1 to be pressed in the event of an error	
	[Disabled]	This option does not require waiting for user intervention in the event of an error. Select this value only if you know the reason why the BIOS error might appear.
	[Enabled]	Enable the BIOS system to wait for "F1" to be pressed in the event of an error at the time of booting
Hit 'DEL' Message Display	Displaying the message "Hit Del to enter Setup" during memory initialization	
	[Disabled]	Displaying the message is disabled
	[Enabled]	Displaying the message is enabled
Interrupt 19 Capture	Capturing the INT19 software interrupt	
	[Disabled]	BIOS will disable additional controllers to capture the INT19 interrupt
	[Enabled]	BIOS will enable additional controllers to capture the INT19 interrupt

5.5 Security

Screen of the "Security" menu and description of menu items are specified below.

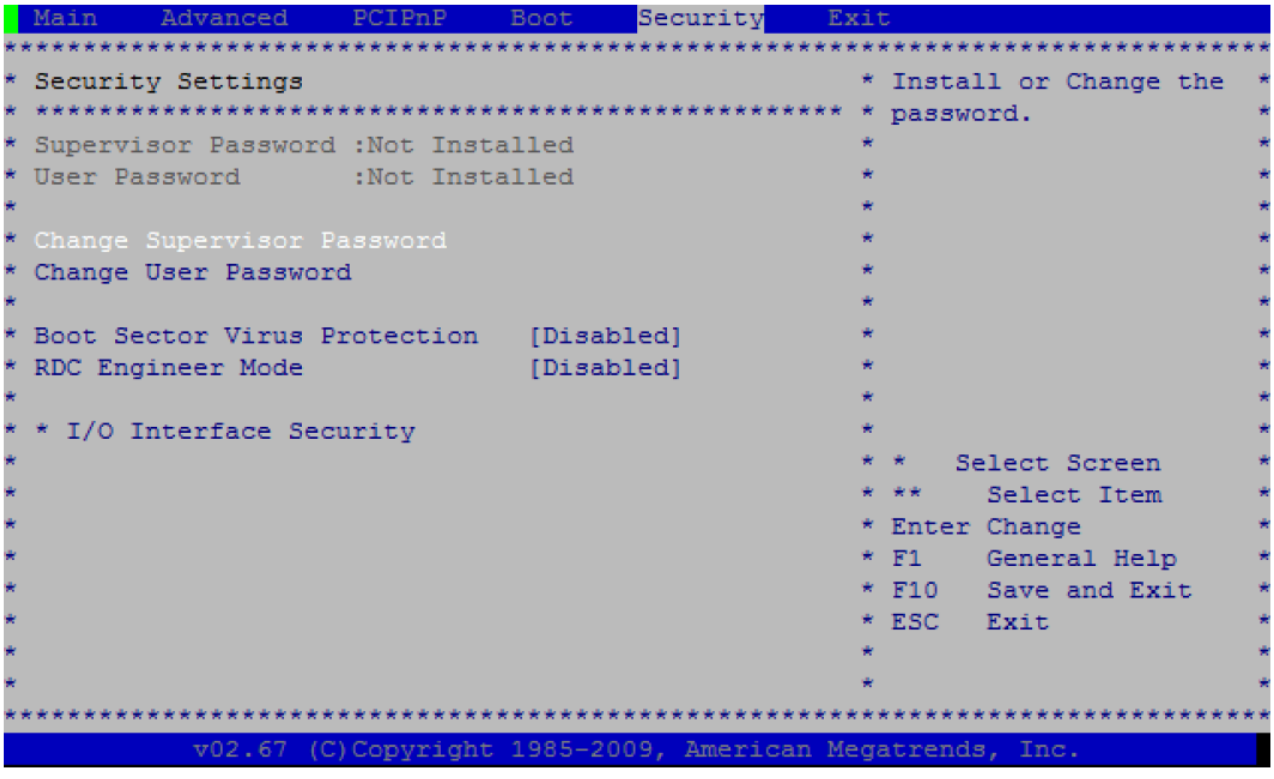


Fig. 5-11 – Screen of the "Security" menu

Table 5-10 – Description of the “Security» menu

Menu item	Purpose	
Change Supervisor Password	Changing the password to allow system boot process (the request is displayed at the time of P.O.S.T.)	
Change User Password	Changing password for accessing to BIOS Setup (requested when entering BIOS Setup)	
Boot Sector Virus Protection	Protection of boot sector against viruses	
	[Disabled]	Selecting this value disables protection of the boot sector against viruses.
	[Enabled]	Selecting the “Enabled” value activates protection of the boot sector against viruses. If any program (or virus) executes the Disk Format command or tries to write to the boot sector on the hard disk, a warning will be displayed on the monitor. While attempting to access the boot sector with protection enabled, the following messages appears: **Boot Sector Write!** **Possible VIRUS: Continue (Y/N)?_** The following message appears after any attempt to format any hard drive via BIOS INT 13 Hard disk drive Service: **Format!!!** **Possible VIRUS: Continue (Y/N)?_**
RDC Engineer Mode	Enable "RDC Engineer Mode". The option appears when you press the F4 key on the keyboard.	
	[Disabled]	The "RDC Engineer Mode" is disabled.
	[Enabled]	The "RDC Engineer Mode" is enabled. When turned on, an additional menu "Strapping Configuration" is displayed in the Advanced section

Submenu “I/O Interface Security” and description of menu items are given below.

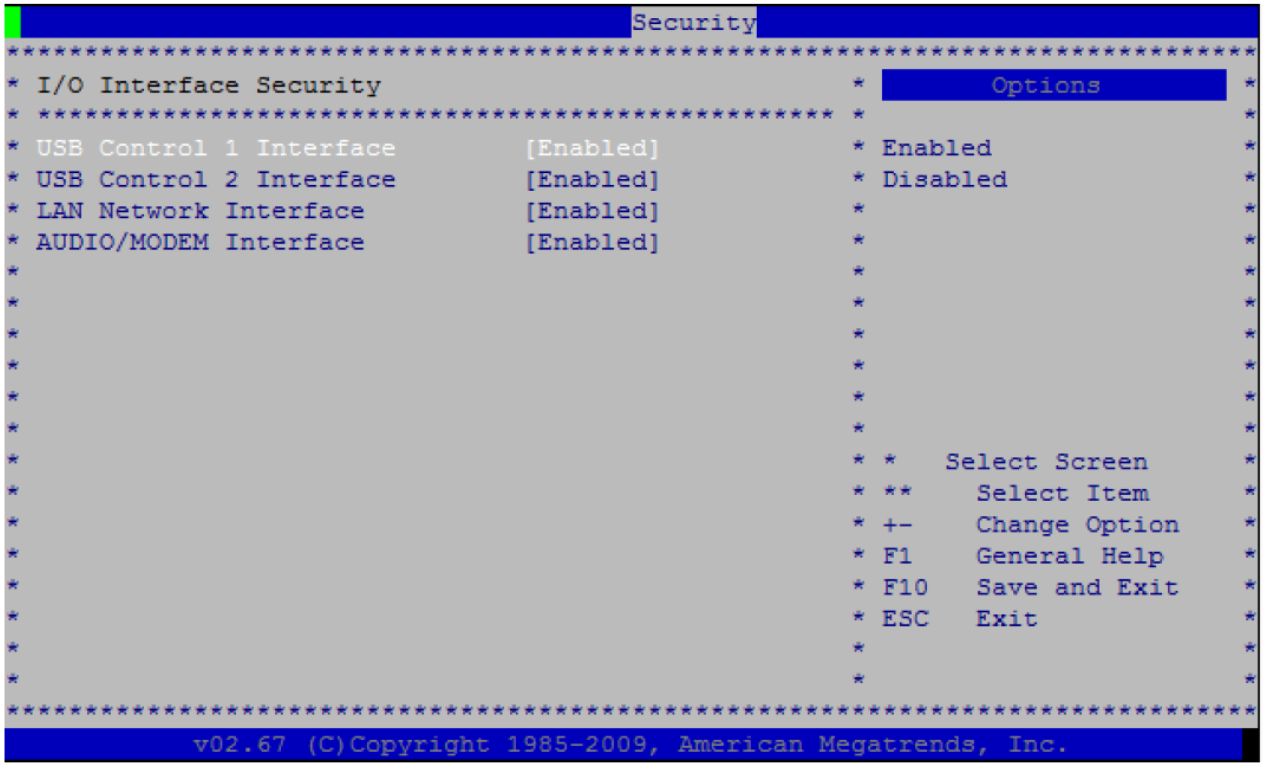


Fig. 5-12 – Screen of the “SouthBridge Configuration” menu

Table 5-11 – Description of the “SouthBridge Configuration” menu

Menu item	Purpose	
USB Control 1 Interface	Controlling operation of the 0th and 1st USB ports	
	[Enabled]	Enable operation of the ports
	[Disabled]	Disable operation of the ports
USB Control 2 Interface	Controlling operation of the 2nd and 3rd USB ports	
	[Enabled]	Enable operation of the ports
	[Disabled]	Disable operation of the ports
LAN Network Interface	Controlling operation of the Ethernet (LAN) integrated controller	
	[Enabled]	Enable operation of the controller
	[Disabled]	Disable operation of the controller
AUDIO/MODEM Interface	[Enabled]	Enable operation of the controller
	[Disabled]	Disable operation of the controller

5.6 Exit

Screen of the “Exit” menu and the relevant description are given below.

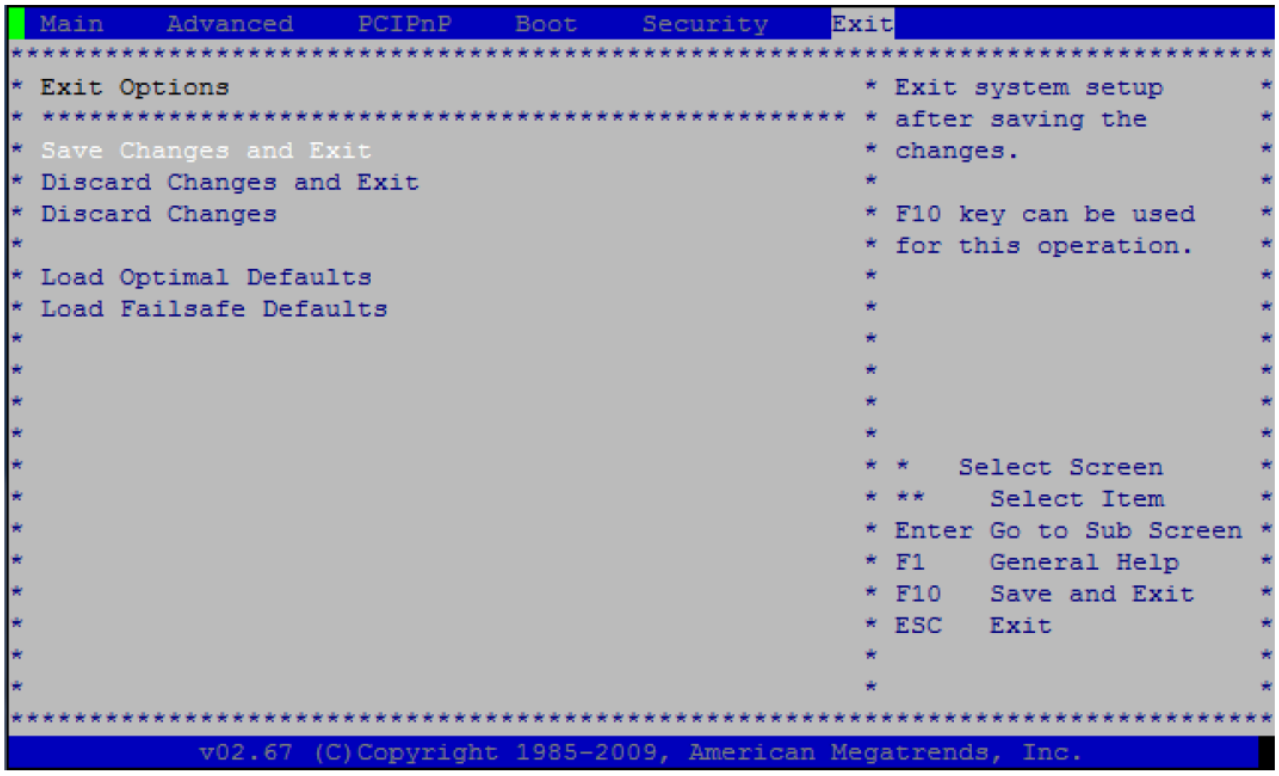


Fig. 5-13 – Screen of the “Exit” menu

Table 5-12 – Description of the “Exit» menu (output)

Menu item	Purpose
Save Changes and Exit	Save settings in the CMOS and FRAM memory and exit BIOS Setup
Discard Changes and Exit	Exit without saving settings to CMOS and FRAM
Discard Changes	Discard the changes made in the settings without exiting BIOS Setup
Load Optimal Defaults	Load optimal (factory) settings without exiting BIOS Setup
Load Failsafe Defaults	Reserved. Same as the loading optimal (factory) settings

ANNEX A

Device programming FAQ

1. Problem with the console via COM-port. You can enter the BIOS Setup, but when DOS starts, it is no longer possible to get there using keyboard via terminal. What is the reason?

The most likely reason for this problem is BIOS Setup. By default, the remote console integrated into the AMI BIOS is enabled only until the BIOS transfers control to the operating system. In order to enable the console I/O integrated into the AMI BIOS, you need to change the BIOS Setup settings - in the “Advanced -> Remote Access Configuration” section, and set the “Redirection after BIOS POST” parameter to “Always” (when the device is delivered, this parameter is set by default in “Boot Loader”). However, it should be noted that the console implemented in the AMI BIOS uses a system timer. You can also use the FreeDOS tools (OS preinstalled by default), such as the **MODE** (change the parameters of I/O devices) and **CTTY** (change the standard I/O device) commands in the AUTOEXEC.BAT file:

```
MODE COMm[:] [BAUD[HARD]=b] [PARITY=p] [DATA=d] [STOP=s]
CTTY COMm
```

COMm – COM- port used (COM1, COM2, COM3, COM4). By default, in the BIOS Setup settings for the COM1 (RS-232) port and for the COM2 (RS-232) port, the base addresses are 3F8h and 2F8h, respectively. In order to use COM1 or COM2 (RS-232) for console I/O, the BAUD parameter must be set properly.

BAUD – baud rate code: 96 – 9600 bit/s, 192 – 19200 bit/s.

BAUDHARD – baud rate code: 96 – 9600 bit/s, 192 – 19200 bit/s, 384 – 38400 bit/s, 1152 – 115200 bit/s.

PARITY – parity (Even, Odd, Mark, Space, None).

DATA – number of data bits (7, 8)

STOP – number of stop bits (1, 2)

Examples of recording in the AUTOEXEC.BAT file:

```
MODE COM1 BAUDHARD=1152 PARITY=NONE DATA=8 STOP=1
CTTY COM1

MODE COM2 BAUD=96 PARITY=NONE DATA=8 STOP=1
CTTY COM2
```

However, it is necessary to consider certain restrictions during the work with the console when the FreeDOS operating system is running (it is preinstalled on the integrated flash drive at the time of delivery), precisely: pressing such keys as “Backspace” and "←", "→" (while no such problems were found when working with MSDOS).

ANNEX B

Terms and abbreviations

Abbreviation	Definition
ACPI	Advanced Configuration and Power Interface
AGP	Accelerated Graphics Port
AGTL	Advanced Gunning Transceiver Logic
BIOS	Basic Input-Output System
DAC	Digital-Analog Converter
DDR SDRAM	Double Data Rate Synchronous Dynamic Random Access Memory
DMA	Direct Memory Access
DMI	Direct Media Interface
DVMT	Dynamic Video Memory Technology
ECC	Error Correction Code
EEPROM	Electrically Erasable Programmable Read-Only Memory
EHCI	Enhanced Host Controller Interface (Universal Serial Bus specification)
EIDE	Enhanced Integrated Drive Electronics
EOS	Electrical Overstress
ESD	Electrostatically Sensitive Device Electrostatic Discharge
FSB	Frequency System Bus

Abbreviation	Definition
FWH	Firmware Hub
GMCH	Graphics and Memory Controller Hub
I²C™	Inter Integrated Circuit
LCD	Liquid crystal display
LPC	Low Pin Count
LVDS	Low Voltage Differential Signal
MDI	Media Dependent Interface
PC	Personal Computer
PIO	Programmed Input/Output
PLCC	Plastic Leaded Chip Carrier
PM	Peripheral Management Controller
POST	Power On Self Test
PSB	Processor System Bus
PWM output	Pulse-Width Modulation

RAMDAC	Random Access Memory Digital-to-Analog Converter
RTC	Real Time Clock
SMB	System Management Bus
Abbreviation	**Definition**
SMBus	System Management Bus
SODIMM	Small Outline Dual In-Line Memory Module
SSD	Solid State Disk
TFT	Thin Film Transistor
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver-Transmitter
UHCI	Universal Host Controller Interface
USB	Universal Serial Bus
UTP	Unshielded Twisted Pair

ANNEX C: DISCLAIMER

This Disclaimer contains special operating conditions of Fastwel in the following areas: intellectual property, warranty policy, conditions of the order and delivery.

1 INTELLECTUAL PRORETY

1.1 If any infraction, interference, improper use, illegitimate exploitation and/or violation of the industrial and/or intellectual property rights of any third party and/or property, exploitation during the use of Fastwel Embedded Module will take place – Fastwel does not guarantee to replace the materials, computer programs, procedures or equipment affected by the complaint and under no circumstances doesn't bear responsibility in any form for possible refusal in case of such a replacement.
1.2 Use of the Fastwel products as well as the objects of intellectual property containing in them, in the ways and for the purposes, not provided by the present user manual and datasheet isn't allowed without preliminary written approval of Fastwel.
1.3 Fastwel is not responsible for possible incidents and losses, related to the operation of end devices, in which the original Fastwel equipment is used.

2 WARRANTY POLICY

2.1 When the detected flaws in an element can be corrected without decreasing the foreseen technical features and functionality for it, User may demand Fastwel the urgent correction of the failures in additionally agreed period and an increasing of the period of the guarantee of the element equal as the time elapsed from the formal request to repair the failures, until the receipt of the repaired element. All costs associated to the correction of failures, included those of assembly, dismantle, transport, tests, etc., if they exist, shall be prosecuted according the Warranty Policy of Fastwel.

3 ORDER AND DELIVERY CONDITIONS

3.1 The general rule is that all Fastwel equipment prices are determined with due consideration of delivery under the EXW terms and conditions (Incoterms 2010). Delivery of the products under other terms and conditions should be preliminary agreed and stated in writing between the parties.
3.2 Unless otherwise expressly agreed with Fastwel, all the deliveries of Fastwel equipment will be carried out only after the official purchase order is obtained and provided that the ordered products have been prepaid in full. Other terms and conditions of cooperation should be made in writing.
3.3 Any delivery of Fastwel electronics is submitted with the right package in accordance with the current rules and standards in the Member States of the European Economic Area. The purchaser independently bears all risks regarding the compliance of package and marking of Fastwel products with legislation requirements being in effect at the place of purchased products destination (in the buyer's country). The specified condition excludes unequivocally any liability of Fastwel for possible non-compliance of package and marking of products with the requirements of legislation of the country of products destination.
3.4 In general, all components of the supply are properly protected with respect to freight, in order to avoid any damage to the supply, third parties, environmental damages or unrelated goods, as consequence of wrong packaging.
3.5 Each package unit is labeled on the exterior area with the indications of product's Part Number and Serial Number.
3.6 The support documents for the order should be made either in English or in Russian unless otherwise agreed between parties in writing.
3.7 Fastwel does not pay penalties and does not cover costs associated with delay in the delivery of the products caused by actions of the third parties, force-majeure etc. - Fastwel doesn't bear any responsibility for non-execution or inadequate execution of the obligations in a case when it is caused by actions of the third parties (for example producers or suppliers of accessories), force majeure etc.
3.8 Fastwel declares that independently and at any time without damage, it has an exclusive right to define and change functionality architecture, bill of materials of its products without any preliminary coordination and approvals of the third parties.

4 OTHER CONDITIONS

4.1 Fastwel has the obligation to respect the current Russian legislation (including, but not limited to environmental, labor, social laws) in each moment and to apply it to its embedded electronics considering all and each execution phase, that is to say, from the design until the commissioning and subsequent maintenance. In this regard Fastwel is not liable to the user or other persons in connection with possible changes of the company's rules (including, but not limited to warranty, ordering policy) caused by changes of the Russian legislation.
4.2 Unless otherwise expressly agreed in writing, Fastwel provides no training for assembly\installation\adjustment\operation of its equipment.