CPC307

PC/104-*Plus*
Vortex86DX Based
CPU Module

User Manual

Rev. 006

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Rev. Index	Brief Description of Changes	Board Index	Date of Issue
001	Initial preliminary version	CPC307 v 2.0	July 2010
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003	Multiple changes caused by changes in the PCB design	CPC307 v 3.1	December 2012
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Safety requirements

This Fastwel Group’s product is developed and tested for the purpose of ensuring compliance to the electric safety requirements. Its design provides long-term trouble-free operation. The service life of the product can be significantly reduced due to the improper handling during unpacking and installation. Therefore, in the interests of your safety and in order to ensure proper operation of the product, you should follow the recommendations below.

Notation Conventions

Warning, ESD Sensitive Device!

This symbol draws your attention to the information related to electro static sensitivity of your product and its components. To keep product safety and operability it is necessary to handle it with care and follow the ESD safety directions.

Warning!

This sign marks warnings about hot surfaces. The surface of the heatsink and some components can get very hot during operation. Take due care when handling, avoid touching hot surfaces!

Caution: Electric Shock!

This symbol warns about danger of electrical shock (> 60 V) when touching products or parts of them. Failure to observe the indicated precautions and directions may expose your life to danger and may lead to damage to your product.

Warning!

Information marked by this symbol is essential for human and equipment safety.
Read this information attentively, be watchful.

Note...

This symbol and title marks important information to be read attentively for your own benefit.

General Safety Precautions

This product was developed for fault-free operation. Its design provides conformance to all related safety requirements. However, the life of this product can be seriously shortened by improper handling and incorrect operation. That is why it is necessary to follow general safety and operational instructions below.

Warning!

All operations on this device must be carried out by sufficiently skilled personnel only.

Warning!

When handling this product, special care must be taken not to hit the heatsink (if installed) against another rigid object. Also, be careful not to drop the product, since this may cause damage to the heatsink, CPU or other sensitive components as well.

Please, keep in mind that any physical damage to this product is not covered under warranty.

Note:

This product is guaranteed to operate within the published temperature ranges and relevant conditions. However, prolonged operation near the maximum temperature is not recommended by Fastwel or by electronic chip manufacturers due to thermal stress related failure mechanisms. These mechanisms are common to all silicon devices, they can reduce the MTBF of the product by increasing the failure probability. Prolonged operation at the lower limits of the temperature ranges has no limitations.

Caution, Electric Shock!

Before installing this product into a system and before installing other devices on it, always ensure that your mains power is switched off.

Always disconnect external power supply cables during all handling and maintenance operations with this module to avoid serious danger of electrical shock.

Unpacking, Inspection and Handling

Please read the manual carefully before unpacking the module or mounting the device into your system. Keep in mind the following:

ESD Sensitive Device!

Electronic modules and their components are sensitive to static electricity. Even a non-perceptible by human being static discharge can be sufficient to destroy or degrade a component's operation! Therefore, all handling operations and inspections of this product must be performed with due care, in order to keep product integrity and operability:

- Preferably, unpack or pack this product only at EOS/ESD safe workplaces. Otherwise, it is important to be electrically discharged before touching the product. This can be done by touching a metal part of your system case with your hand or tool. It is particularly important to observe anti-static precautions when setting jumpers or replacing components.
- If the product contains batteries for RTC or memory back-up, ensure that the module is not placed on conductive surfaces, including anti-static mats or sponges. This can cause short-circuit and result in damage to the battery and other components.
- Store this product in its protective packaging while it is not used for operational purposes.

Unpacking

The product is carefully packed in an antistatic bag and in a carton box to protect it against possible damage and harmful influence during shipping. Unpack the product indoors only at a temperature not less than +15°C and relative humidity not more than 70%. Please note, that if the product was exposed to the temperatures below 0°C for a long time, it is necessary to keep it at normal conditions for at least 24 hours before unpacking. Do not keep the product close to a heat source.

Following ESD precautions, carefully take the product out of the shipping carton box. Proper handling of the product is critical to ensure correct operation and long-term reliability. When unpacking the product, and whenever handling it thereafter, be sure to hold the module preferably by the front panel, card edges or ejector handles. Avoid touching the components and connectors.

Retain all original packaging at least until the warranty period is over. You may need it for shipments or for storage of the product.

Initial Inspection

Although the product is carefully packaged, it is still possible that shipping damages may occur. Careful inspection of the shipping carton can reveal evidence of damage or rough handling. Should you notice that the package is damaged, please notify the shipping service and the manufacturer as soon as possible. Retain the damaged packing material for inspection.

After unpacking the product, you should inspect it for visible damage that could have occurred during shipping or unpacking. If damage is observed (usually in the form of bent component leads or loose socketed components), contact Fastwel's official distributor from which you have purchased the product for additional instructions. Depending on the severity of the damage, the product may even need to be returned to the factory for repair. DO NOT apply power to the product if it has visible damage. Doing so may cause further, possibly irreparable damage, as well as result in a fire or electric shock hazard.

If the product contains socketed components, they should be inspected to make sure they are seated fully in their sockets.

Handling

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

In order to keep Fastwel's warranty, you must not change or modify this product in any way, other than specifically approved by Fastwel or described in this manual.

Technical characteristics of the systems in which this product is installed, such as operating temperature ranges and power supply parameters, should conform to the requirements stated by this document.

Retain all the original packaging, you will need it to pack the product for shipping in warranty cases or for safe storage. Please, pack the product for transportation in the way it was packed by the supplier.

When handling the product, please, remember that the module, its components and connectors require delicate care. Always keep in mind the ESD sensitivity of the product.

Three Year Warranty

Fastwel Co. Ltd. (Fastwel), warrants that its standard hardware products will be free from defects in materials and workmanship under normal use and service for the currently established warranty period. Fastwel's only responsibility under this warranty is, at its option, to replace or repair any defective component part of such products free of charge.

Fastwel neither assumes nor authorizes any other liability in connection with the sale, installation or use of its products. Fastwel shall have no liability for direct or consequential damages of any kind arising out of sale, delay in delivery, installation, or use of its products.

If a product should fail through Fastwel's fault during the warranty period, it will be repaired free of charge. For out of warranty repairs, the customer will be invoiced for repair charges at current standard labor and materials rates.

Warranty period for Fastwel products is 36 months since the date of purchase.

For custom-made products, the warranty period is 60 months from the date of sale (unless otherwise specified in the supply agreement).

The warranty set forth above does not extend to and shall not apply to:

1. Products, including software, which have been repaired or altered by other than Fastwel personnel, unless Buyer has properly altered or repaired the products in accordance with procedures previously approved in writing by Fastwel.
2. Products, which have been subject to power supply reversal, misuse, neglect, accident, or improper installation.

Returning a product for repair

1. Apply to Fastwel company or to any of the Fastwel's official representatives for the Product Return Authorization.
2. Attach a failure inspection report with a product to be returned in the form, accepted by customer, with a description of the failure circumstances and symptoms.
3. Carefully package the product in the antistatic bag, in which the product had been supplied. Failure to package in antistatic material will VOID all warranties. Then package the product in a safe container for shipping.
4. The customer pays for shipping the product to Fastwel or to an official Fastwel representative or dealer.

1 Introduction

1.1 Purpose of the device

This User Manual (hereinafter referred to as the User Manual or UM) presents general information on CPC307 CPU module (hereinafter referred to as the module), the details of its proper and safe installation, configuration and operation. The issues of PC/104 modules and external devices connection are also considered.

Based on x86-compatible 32-bit Vortex86DX System-on-Chip (SoC) operating at 600 MHz. The module is made in PC/104-plus format and designed for embedded applications that require CAN interfaces, high-speed RS-422/485 and RS-232 ports, low power consumption in the operating temperature range from - 40 to +85 ºC.

The module functionality can be expanded by connecting additional modules - PC/104 and PC/104-plus expansion boards depending on the module version.

The User Manual provides instructions on correct and safe installation, power-up and configuration of the module, connection and interaction with expansion modules or external devices.

The User Manual also describes how to start, debug and use the programs from the basic and service software (hereinafter referred to as the Software), as well as BIOS backup features for module versions 3.x and older versions.

1.2 CPC307 Versions, delivery checklist, ordering information

1.2.1 Versions and ordering information

The versions and designations of the module are specified in Table 1.1.

Table 1.1: Module configuration depending on the module versions

Name	Designation	Ordering name	Description
CPC307 CPU Module	CPC307	CPC307-02	Vortex86DX (600 MHz), 256 MB RAM, flash drive - 1 GB – for module versions up to 4.x; 2 GB – for module versions 4.x, IDE, 2xRS-232/485/422, 2xRS232, 2xRS-422/485, 2xCAN, LAN 10/100, LPT, 4xUSB2.0, 8xGPIO, 2xI2C, PC/104-*plus* (ISA, PCI) format.
		CPC307-03	Vortex86DX (600 MHz), 256 MB RAM, flash drive - 1 GB – for module versions up to 4.x; 2 GB – for module versions 4.x, IDE, 2xRS-232/485/422, 2xRS232, LAN 10/100, LPT, 4xUSB2.0, 8xGPIO, 2xI2C, PC/104-*plus* (ISA, PCI) format.
		CPC307-04	Vortex86DX (600 MHz), 256 MB RAM, 2x microSD, IDE, 2xRS-232/485/422, 2xRS-232, 2xRS-422/485, 2xCAN, LAN 10/100, LPT, 4xUSB2.0, 8xGPIO, 2xI2C, PC/104-*plus* (ISA, PCI) format.
		CPC307-05	Vortex86DX (600 MHz), 256 MB RAM, flash drive 1 GB – for versions up to 4.x; 2 GB – for module versions 4.x, IDE, 2xRS-232/485/422, 2xRS232, 2xRS-422/485, 2xCAN, LAN 10/100, LPT, 4xUSB2.0, 8xGPIO, 2xI2C, PC/104-*plus* (ISA, PCI) format, COATED, from -50 up to +90 ºC

Options available for CPC307:

\COATED – Protective coating option (for CPC307-02, -03, -04 versions);
\LNX – Preinstalled Linux 2.6 (for CPC307-02, -03, -05);

Pre-installation on special order (for modules CPC307-02,-03,-05):
\WCE5 – Windows CE 5.0
\QNX – QNX 6.4

1.2.2 Delivery checklist

Table 1.2 contains delivery checklist for all the module versions.

Table 1.2. Delivery checklist of the module

Name	Designation	Description	Number
IMES.467444.038	CPC307	CPC307 CPU Module	1 pcs
IMES.467941.010		Set of mounting parts consisting of:	1 pcs
FAPI.685611.082	ACS00023	Adapter cable IDC2-10 2 mm – DB9M for connecting COM-port	1 pcs
–	–	M3 nut DIN934	4 pcs
–	–	PCSN-15 rack for printed circuit boards, brass	4 pcs
–	–	Toothed lock washer Ø3 DIN6798A	4 pcs
IMES.467941.010	Packaging	PC104 box 155x140x45 mm	1 pcs

Table 1.3 shows a list of optional accessories for the CPC307 module, which are not included in the delivery checklist and can be purchased additionally.

Table 1.3. Additional accessories for CPC307

Designation	Ordering name	Description
CDM02	CDM02	Adapter for connecting a 3.5” HDD
FC44	ACS00010	Cable with 44 pins with 2 mm pitch to connect a 2.5" HDD
ACS00023	ACS00023	Cable IDC2-10 - D-SUB 9M (plug, two-row, in the enclosure) to connect to the RS-232 ports

Designation	Ordering name	Description
ACS00031-03, ACS0054	ACS00031-03, ACS0054	Includes JST PHR-2 connector and SPH-002T-P0.5S pin set or 0.5 m crimped wire connector. Recommended mating part for the XP19 connector (opto-isolated reset/interrupt)
ACS00038, ACS00038-01, ACS00038-02	ACS00038, ACS00038-01, ACS00038-02	Power socket with single pins (ACS00038) or crimped wire length of 1 m (ACS00038-01,-02). Recommended mating part for the XP22 connector (Additional power connector)
ACS00040-01	ACS00040-01	2mm IDC2-10 socket (Leotronics). Recommended mating part for XP5 (CAN), XP6 (COM3), XP7 (COM4), XP9 (LAN), XP10 (COM1), XP14 (GPIO), XP16 (COM2), XP17 (COM5,6)
ACS00048, ACS00049, ACS00049-02	ACS00048, ACS00049, ACS00049-02	Insert (socket, Leotronics) for 10 positions, with a pin pitch of 2 mm and a set of individual pins (ACS00049) or crimped wire with a length of 1 m (ACS00049-02). Recommended mating part for XP5 (CAN), XP6 (COM3), XP7 (COM4), XP9 (LAN), XP10 (COM1), XP14 (GPIO), XP16 (COM2), XP17 (COM5,6)
ACS00040-05	ACS00040-05	IDC2-44 2 mm socket (Leotronics). Recommended mating part for XP12 (LPT, USB), XP13 (IDE) connectors.
ACS00048-04, ACS00049, ACS00049-02	ACS00048-04, ACS00049, ACS00049-02	Insert (socket, Leotronics) for 44 positions, with a pin pitch of 2 mm and a set of individual contacts (ACS00049) or crimped to a wire length of 1 m (ACS00049-02). Recommended mating part for XP12 (LPT, USB), XP13 (IDE) connectors.
ACS00042	ACS00042	Null-modem cable
ACS00043-01	ACS00043-01	PS/2 cable. Used to connect PS/2 devices to XP23 connector.
ACS00051	ACS00051	Cable for connecting two standard USB devices to XP12 (LPT/USB) connector.

Table 1.4. Differences among the supplied configurations

Ordering number	IDE	LAN	CAN	COM	GPIO	I2C	Format	Coating
CPC307-02	ATA Flash Disk (soldered, 1 GB for versions before 4.x; 2 GB – for versions 4.x)	LAN	CAN 1-2	COM 1-6	GPIO	I2C	PC104-plus (ISA, PCI)	
CPC307-03	ATA Flash Disk (soldered, 1 GB for versions before 4.x; 2 GB – for versions 4.x)	LAN		COM 1-4	GPIO	I2C	PC104-plus (ISA, PCI)	
CPC307-04	microSD 1-2	LAN	CAN 1-2	COM 1-6	GPIO	I2C	PC104-plus (ISA, PCI)	
CPC307-05	ATA Flash Disk (soldered, 1 GB for versions before 4.x; 2 GB – for versions 4.x)	LAN	CAN 1-2	COM 1-6	GPIO	I2C	PC104-plus (ISA, PCI)	Conformal coating, from - 50 to +90 ◦C

2 Technical Specifications

2.1 General information on module functionality

- CPU: Integrated in DM&P Vortex86DX SoC
  - 600 MHz
  - 32-bit x86 compatible core
  - 16-bit memory bus
  - Math coprocessor
  - 32 KB L1, 256 KB L2 cache
  - 6-stage pipeline
- System memory256 MB soldered DDR2 SDRAM:
  - bus frequency 266 MHz *for module versions lower than 4.x;*
  - bus frequency 333 MHz *for module versions 4.x.*
- Connection of HDD and optical disc drive for DVD/CD:
  - 2 x connectors for microSD cards (only for CPC307-04, ATA Flash Disk is not installed);
  - For other module versions connection of one additional IDE device is available;
  - Ultra-DMA2 mode support;
- Flash memory
  - *For module versions before 4.x*: 1 GB, using NAND technology (via ATA Flash disk controller) for -02, -03, -05 versions. Space available to the user: 870 MB;
  - For module versions 4.x: 2 GB, using NAND technology (via ATA Flash disk controller) for -02, -03, -05 versions. Space available to the user: 1870 MB;
  - SD controller: connection of up to two microSD cards up to 4 GB (for -04 version).
  - PS/2 keyboard and mouse port.
  - Opto-isolated reset/interrupt, isolation voltage not less than 500 V.
- USB port:
  - Supports up to 4 x USB 1.1 devices, USB 2.0;
  - Supports booting from USB devices;
- Ethernet 10/100 Mbit controller, isolation voltage not less than 500 V;
- Serial ports:
  - COM1, COM2: RS-232/422/485, up to 115.2 kbaud, full;
  - COM3, COM4: RS-232, up to 115.2 kbaud, full;
  - COM5, COM6: RS-422/485, up to 3.6 Mbaud, channel-to-channel isolation, isolation voltage at least 500 V;
  - Console input/output via serial port (COM1 to COM4).
- Two CAN 2.0b interfaces, SJA1000T controller, baud rate up to 1 Mbit/s, per channel isolation, isolation voltage at least 500 V;
- Universal parallel port (LPT) with support for SPP, EPP, ECP modes;
- PCI-104 bus (PCI);

- PC-104 bus (ISA);
- GPIO port, 8 digital I/O lines;
- Two I2C ports (combined with GPIO port);
- 3 x watchdog timers:
  - 2 x with software control capability, integrated into the Vortex86DX SoC;
  - Hardware timer with a fixed 1.6 s interval;
- Flash BIOS:

  - For module versions before 4.x:
  - 512 Kbyte parallel Flash (ISA);
  - 256 Kbyte (backup, SPI Flash);
  - Modifiable within the system;
  - Option to automatically reboot from the BIOS backup;

  - For 4.x module versions:
  - 256 Kbytes (SPI Flash) without BIOS backup;
  - BIOS hardware reset option;
- Real-time clock;
- 256 byte of CMOS RAM and 256 KB of non-volatile FRAM (SPI) memory:
  - Automatic saving and retrieval of CMOS memory settings when the module is operated without a replaceable DC battery installed;
  - Write/read user data via BIOS functions.
- Software compatibility:
  - MS DOS 6.22;
  - FreeDOS;
  - Windows CE 5.0;
  - Linux 2.6;
  - QNX 6.4;

2.2 Power Requirements

The module's power supply must comply with the requirements given in Table 2.1.

The module is powered via the PC/104 and PC/104-plus connector (if installed). If an external power supply is required, an additional XP22 power connector (4-pin AMP 4-171826-4 connector) can be used.

For versions 3.x and below, the starting current of the module is 2.1 A for the CPC307-02 version. The power supply source must be capable of providing the starting current. A power supply source with a current limiting mode of at least 1.2 A can be used. When selecting a power supply, the starting current and the current consumption of the expansion modules must be taken into account.

The module version 4.0 and higher have a "soft" start mechanism. The module's power-up delay after applying power is about 200 ms (max). To ensure a certain level on the I/O port lines within 200 ms after power-up, additional measures must be taken.

Attention!

It is recommended to take additional measures to ensure protection of external devices against "+5 V" conductive interference in case of using one voltage output of the power supply.

Consumption current typical value is 0.6 A.

Table 2.1: Power Supply Requirements

Connectors	Power Voltage	Voltage limits	Maximum load current	Starting current
PC/104 и PC/104-*plus*	+5 V	From +4.75 to +5.25V	1A	2.1 (0.5 ms) – for module versions lower than 4.x. 2.5 (0.5 ms) – for module versions 4.x.
Additional power supply connector	+5 V	From +4.75 to +5.25V	1A	2.1 (0.5 ms) – for module versions lower than 4.x. 2.5 (0.5 ms) – for module versions 4.x.

2.3 Operating conditions

Modules must be resistant to ambient air temperature changes in the range according to Table 2.2 at relative humidity up to 80 %, non-condensing, according to the GOST 28209-89 standard. Modules with conformal coating must be resistant to cyclic damp heat at ambient air temperature + (55 ± 2) °C, relative humidity (93 ± 3) % in accordance with the GOST 28216-89 standard.

Table 2.2. Ranges of ambient air temperature changes

Version by temperature range	Module	Lower range value, ºC	Higher range value, ºC
Industrial temperature range	CPC307-02/03/04	- 40	+ 85
	CPC307-05	- 50	+ 90

Modules storage conditions 1 according to the GOST 15150-69 standard.

2.4 Mechanical

- Vibration (5 ... 2000 Hz) – 10g;
- Single shock, peak acceleration – 150 g;
- Multiple shock, peak acceleration – 50 g.

If the module is operated in harsh environment, it is recommended to additionally fix counterpart connectors and cables.

2.5 Dimensions and Weight

The module weight should not exceed the values specified in Table 2.3.

2.3. Module weight

Version	Net weight in kg, max	Gross weight in kg, max
CPC307-02	0.125	0.265
CPC307-03	0.120	0.260
CPC307-04	0.125	0.265
CPC307-05	0.135	0.275

The overall dimensions of the versions and the location of the components are shown in Figure 2.1.

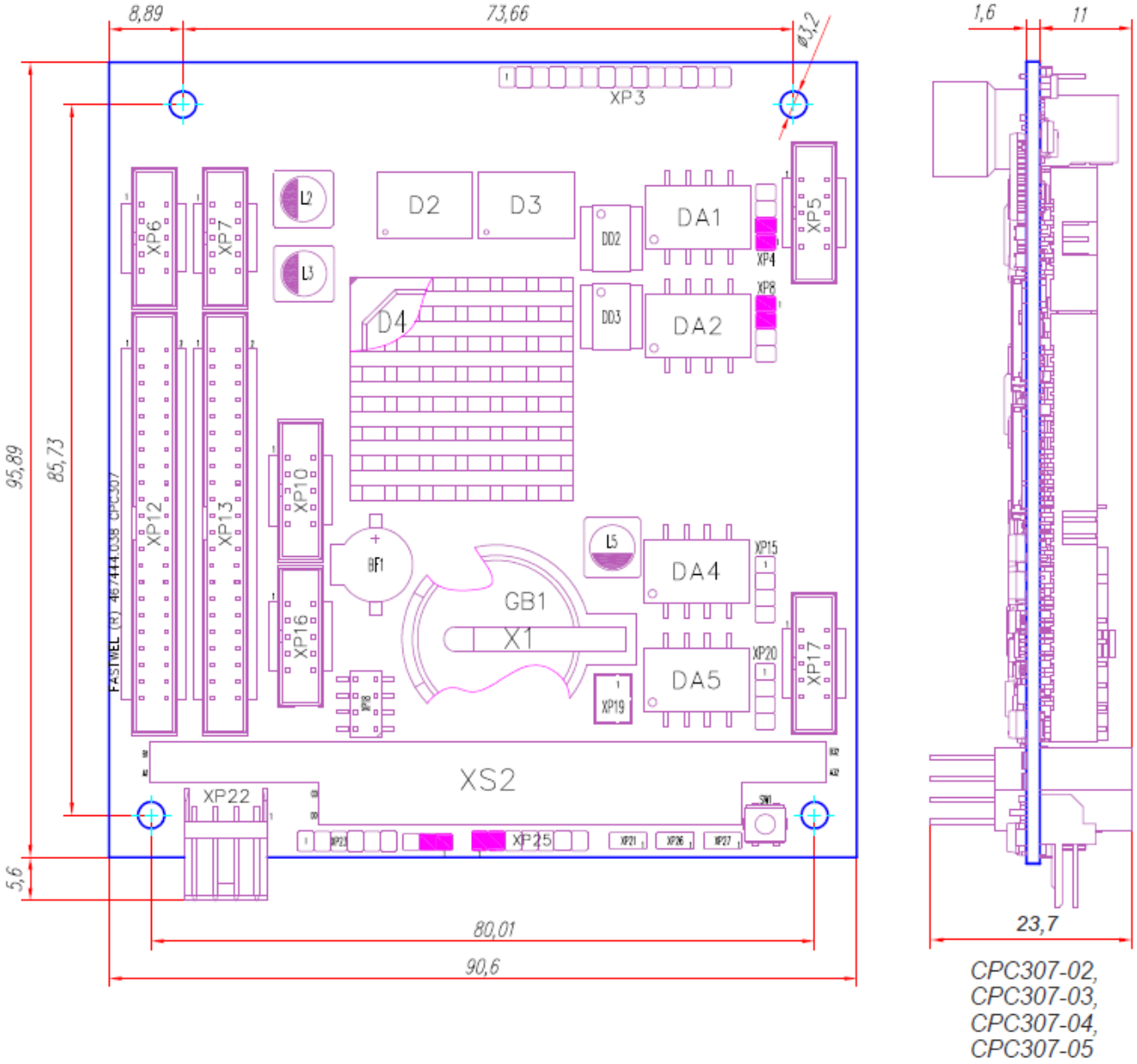


Figure 2.1 a) Overall dimensions of the CPC307 components and their locations (this figure is valid for versions 3.x)

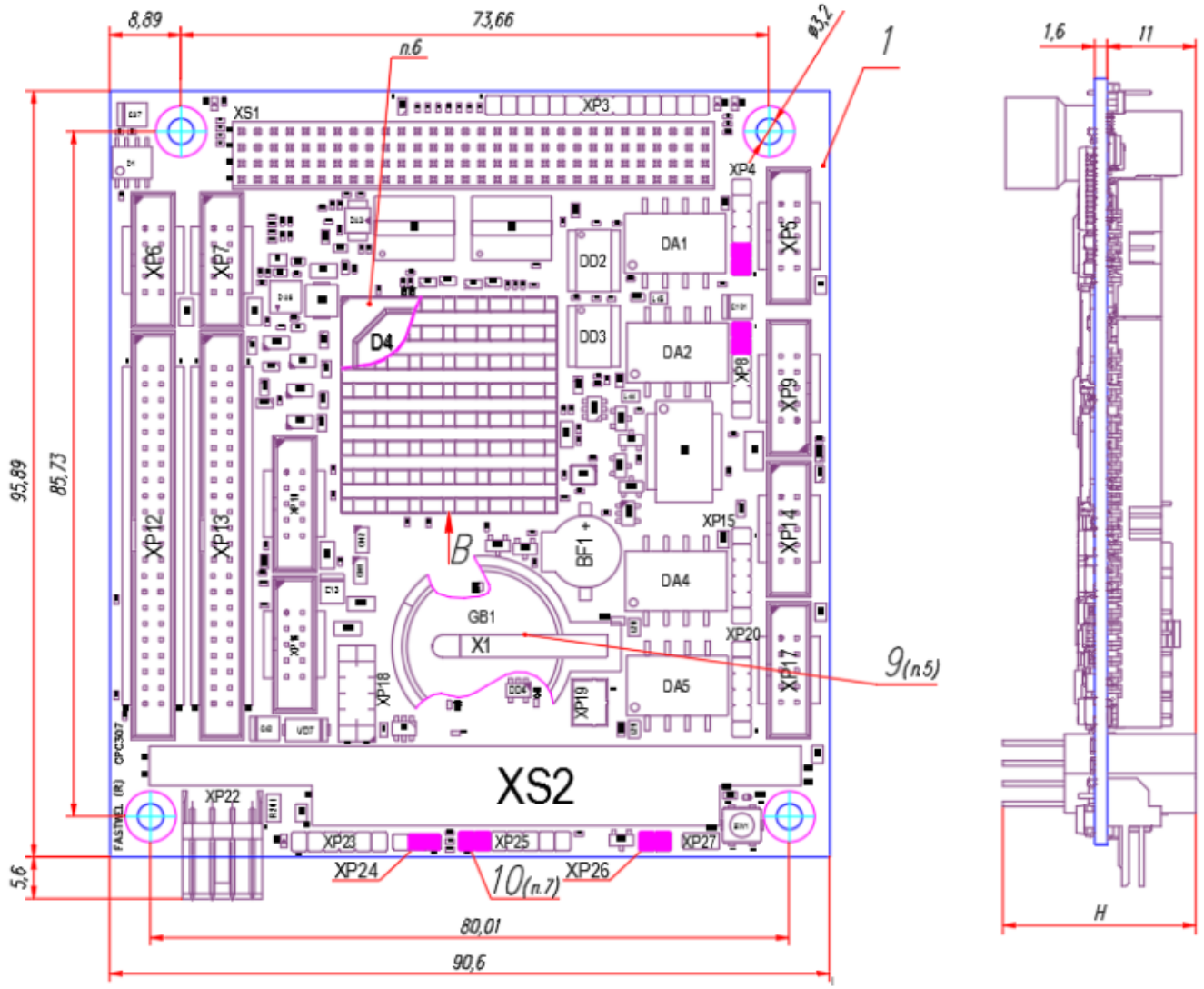


Figure 2.2 b) Overall dimensions of the CPC307 components and their locations (this figure is valid for versions 4.x)

2.6 MTBF

The MTBF value amounts to 200,000 hours.

This MTBF value is calculated according to: Telcordia Issue 1 model, Method I Case 3, for continuous operation at a surface location and at the environmental conditions corresponding to the moderately cold climate in according with the GOST 15150-69 standard and at ambient temperature of +30°C.

3 Intended use of the module

A diagram showing the connection of the necessary devices to the module is shown in Figure 3.1.

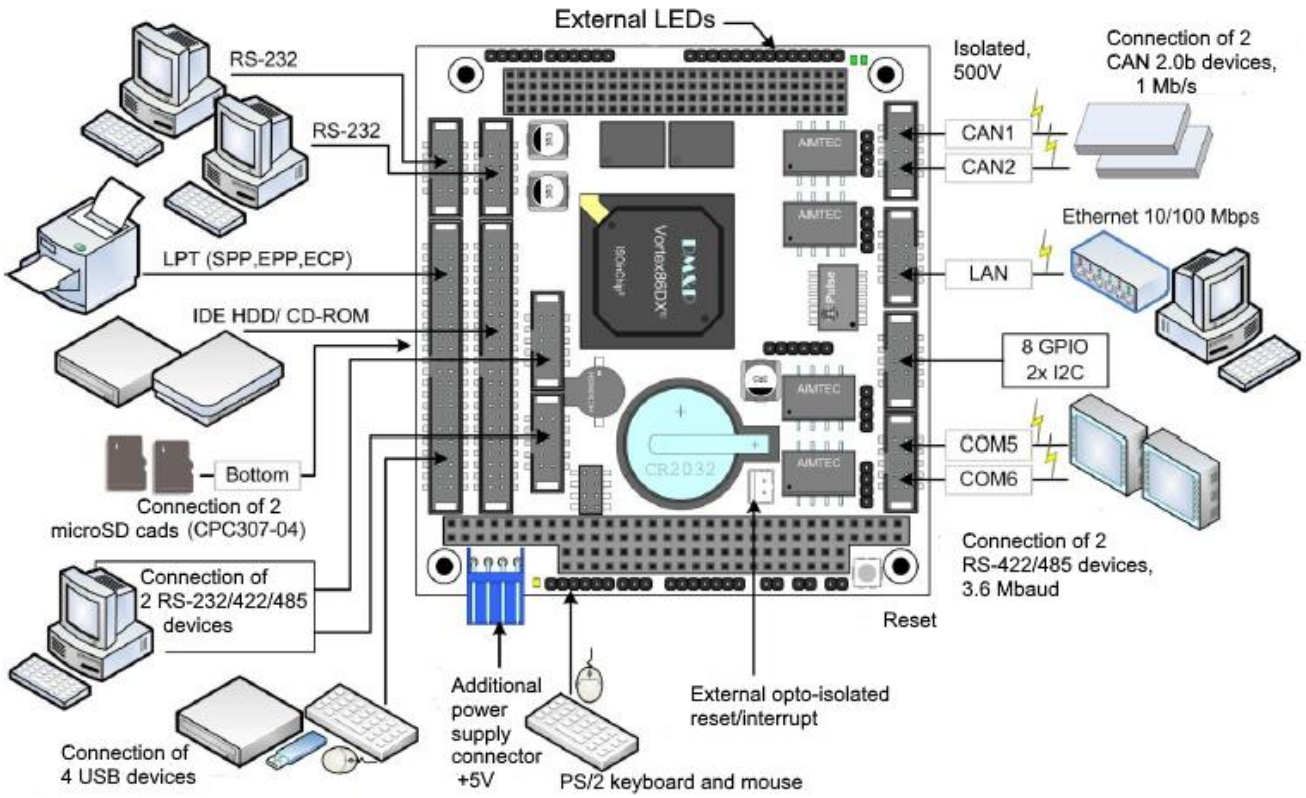


Figure 3.1. Connection of external devices to the CPC307

The devices necessary for module power on and testing its functionality are:
- a power supply source with +5 V output voltage and at least 2.1 A current connected to the PC/104 connector or to the XP22 auxiliary power connector;

- a console PC operating in terminal emulation mode can act as a display device. One of the RS-232 interfaces can serve as the console port (to do so you must select the appropriate port in the BIOS Setup menu). Console I/O port is preset to COM1 (RS-232 mode) with the parameters 115200, 8, n, 1. The default mode of the console is only input/output messages regarding the POST (Power On Self Test) procedure passing. If you need to work with the operating system through the integrated console, you must change the mode of the console Redirection After BIOS POST="Always", Terminal Display Mode="Recorder Mode" in the BIOS Setup menu. The more detailed description of the console settings are given in Section 5.2.3 Remote Access Configuration (Console I/O settings).

– The CPC307-02,-03,-05 modules come with the FreeDOS operating system preinstalled on an ATA flash drive.

4 Device and operation

4.1 Structure and Layout of main elements

The module's block diagram is shown in Fig. 4. 1.

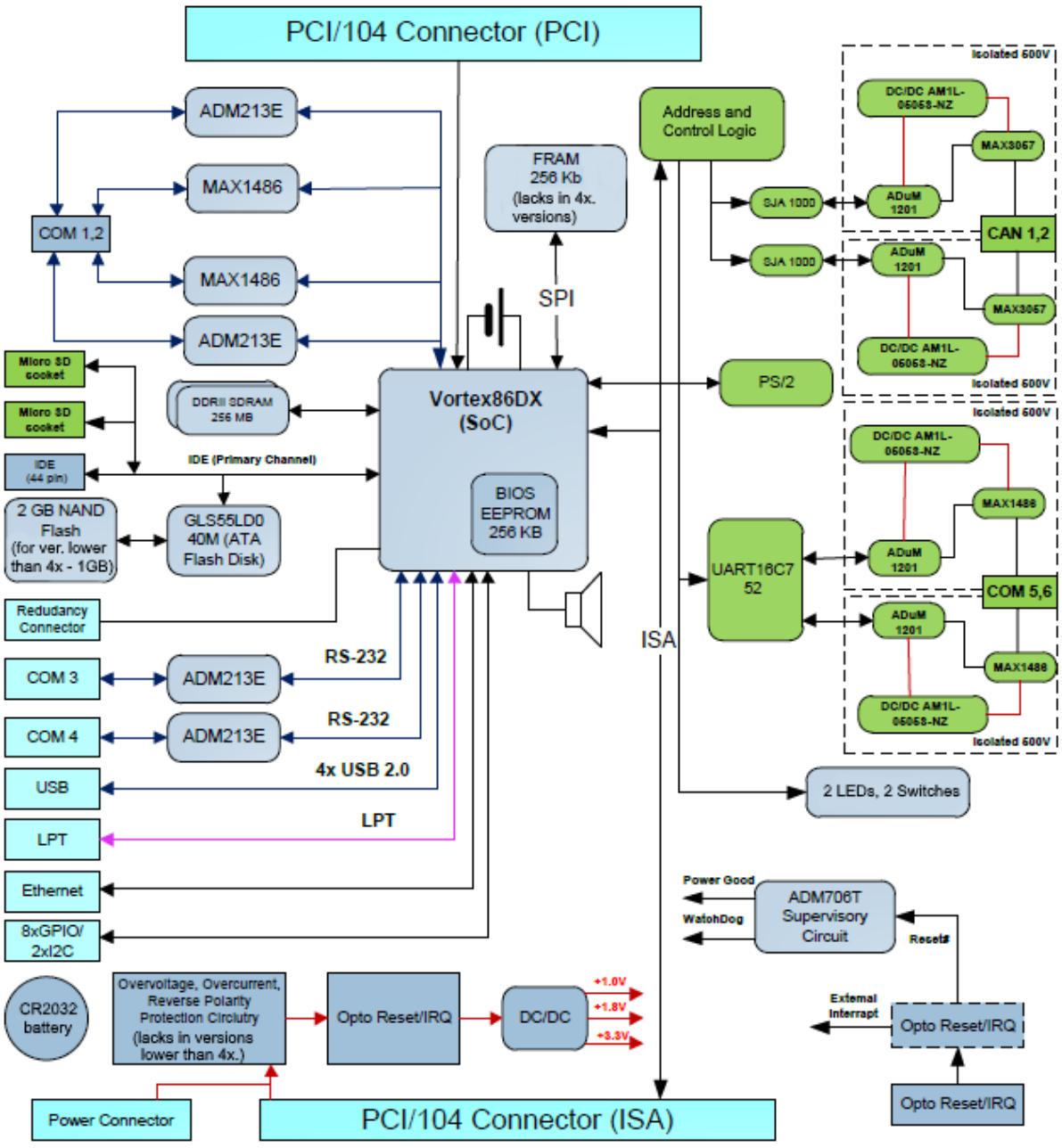


Figure 4.1: CPC307 Block Diagram

CPC307 includes the following main functional units:

- SoC Vortex86DX
- 256 MB soldered DDR2 SDRAM system memory;
- IDE port with support for up to two UltraDMA/100 devices;
- SD controller (IDE);
- Onboard NAND flash-disk (IDE);
- PS/2 keyboard/mouse port;
- Optoisolated external reset//interrupt signal, isolation voltage min.500V;
- 4 x USB 2.0 channels;
- Fast Ethernet port, 10/100 Mbit/s, isolation voltage min. 500V (except for CPC307-01);
- Serial ports:
  - COM1: RS-232/422/485, up to 115.2 Kbaud, complete;
  - COM2: RS-232/422/485, up to 115.2 Kbaud, complete;
  - COM3: RS-232, up to 115.2 Kbaud, complete;
  - COM4: RS-232, up to 115.2 Kbaud, complete;
  - COM5: RS-422/485, up to 3.6 Mbaud, isolation voltage min.500 V;
  - COM6: RS-422/485, up to 3.6 Mbaud, isolation voltage min.500 V;
  - Console I/O via the serial port (COM1 – COM4).
- CAN:
  - Two CAN 2.0b ports, SJA1000T controller; data transfer rate: up to 1 Mbit/s; 500 V isolation;
- Universal parallel port (LPT), support of the SPP/ECP/EPP modes;
- PCI-104 (PCI) bus;
- PC-104 (ISA) bus;
- GPIO port, 8 digital I/O lines;
- Two I2C ports, via GPIO port;
- Three watchdog timers:
  - One with fixed timeout period of 1.6 s;
  - Two integrated into Vortex86DX with programmable control;
- Flash BIOS chip;

  For 4x versions:
  - 512 KB, parallel Flash (ISA);
  - 256 KB (reserve copy, SPI Flash);
  - Modifiable within the system;
  - Option of an automatic reboot from the BIOS reserve copy;

  For versions older than 4x.:
  - 256 KB (SPI Flash) without BIOS reserve copy,
  - BIOS hardware reset option;
- Real time clock;
- 256 byte CMOS RAM and 256 KB non-volatile FRAM (SPI) memory for configuration storage;
- The location of the main components, connectors, terminals strips for the component side (TOP) and the mounting side (BOTTOM) is shown in Figure 4. 2 – Figure 4. 6 for different versions of the module.

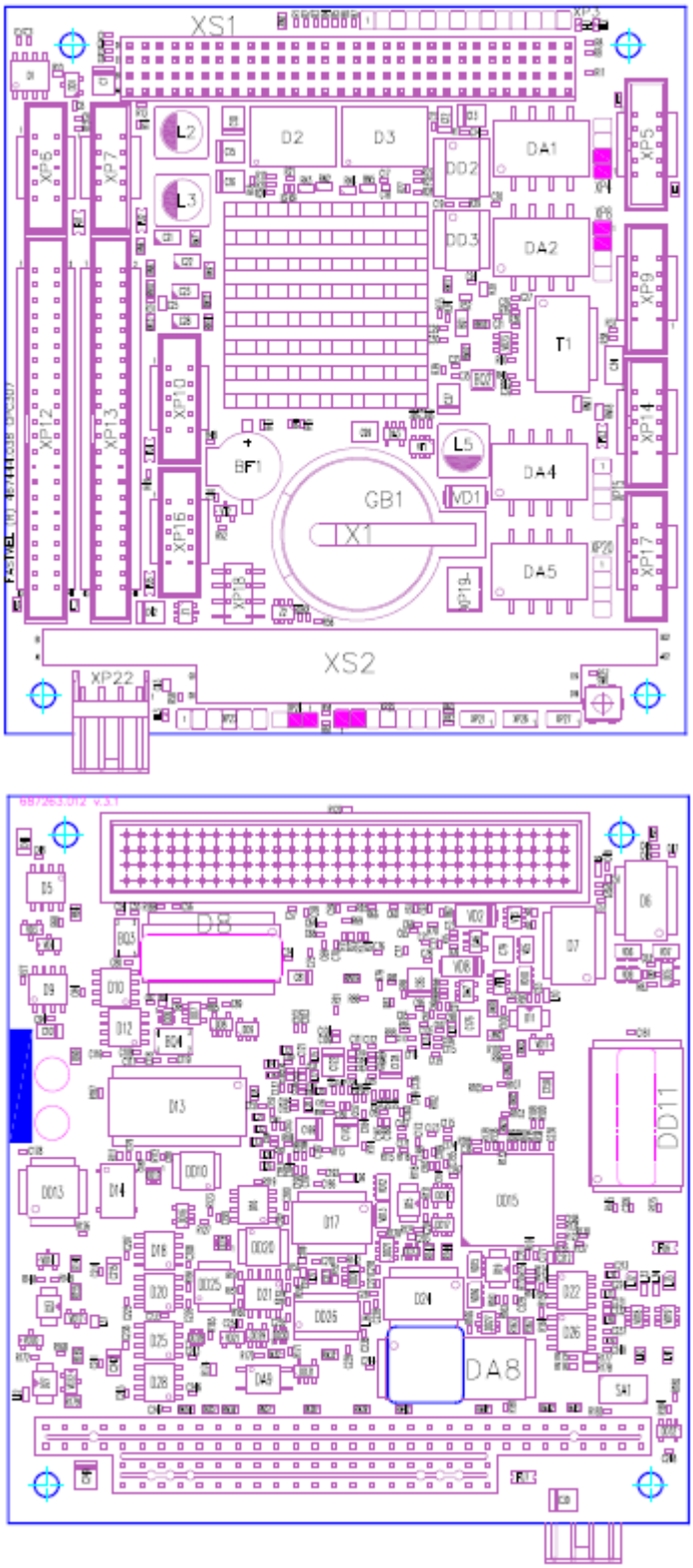


Figure 4. 2 a) Location of connectors and main components on the TOP and BOTTOM for the CPC307-02, CPC307-05 versions (valid for CPC307 v.3.x)

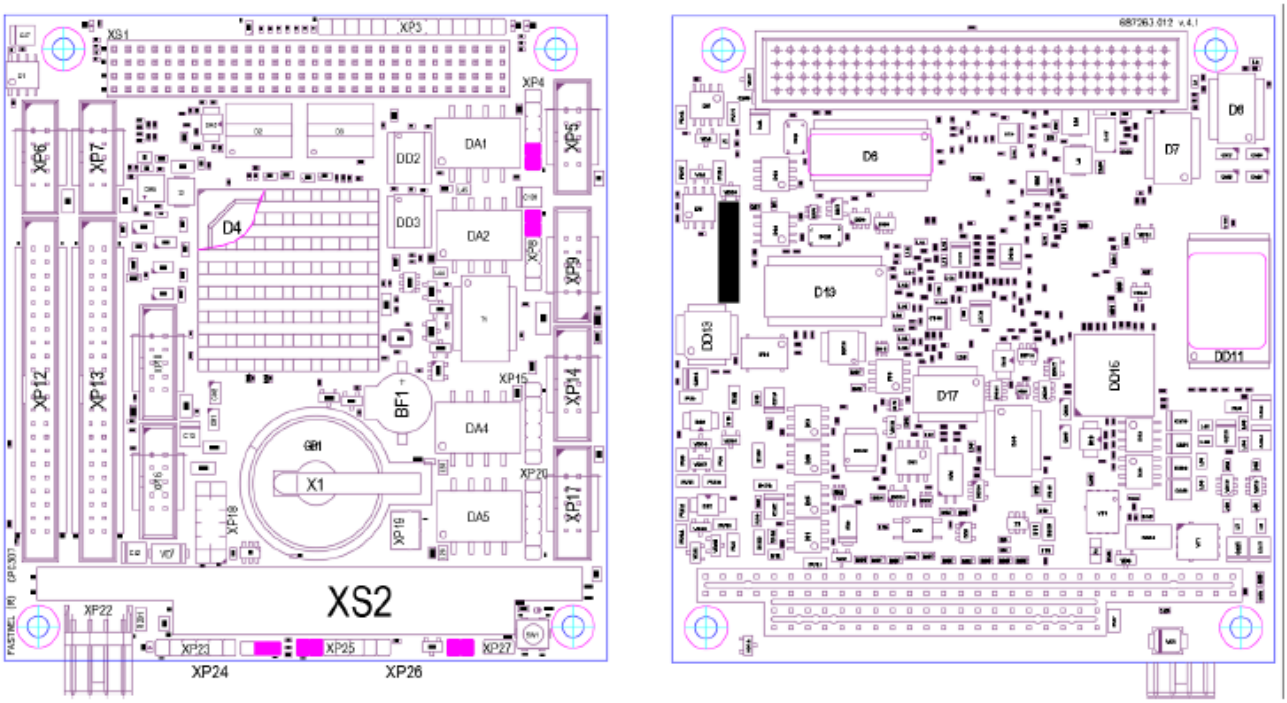


Figure 4.3 b) Location of connectors and main components on the TOP and BOTTOM sides of the CPC307-02, CPC307-05 versions (relevant to CPC307 v.4.x)

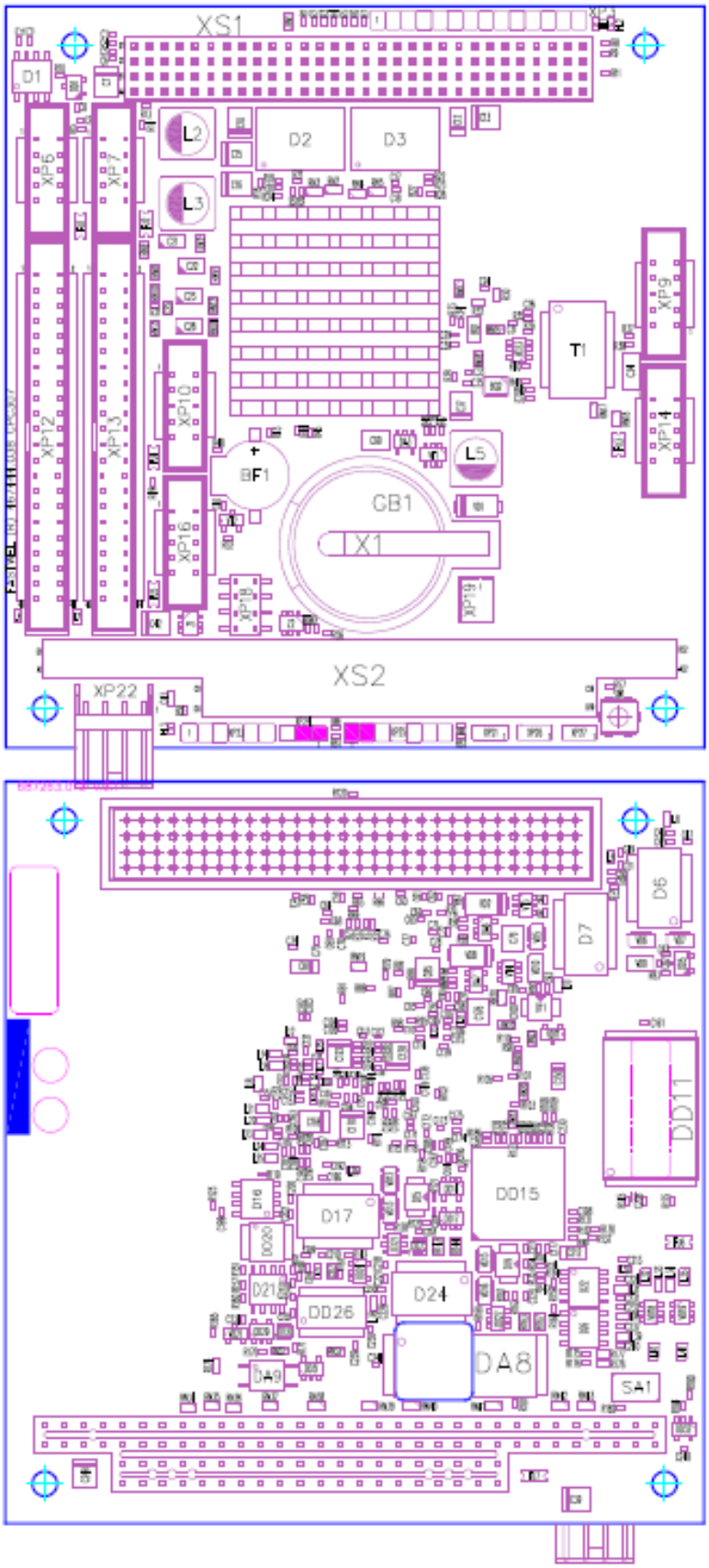


Figure 4.4 a) Location of connectors and main components on the TOP and BOTTOM for the CPC307-03 version (valid for CPC307 v.3.x)

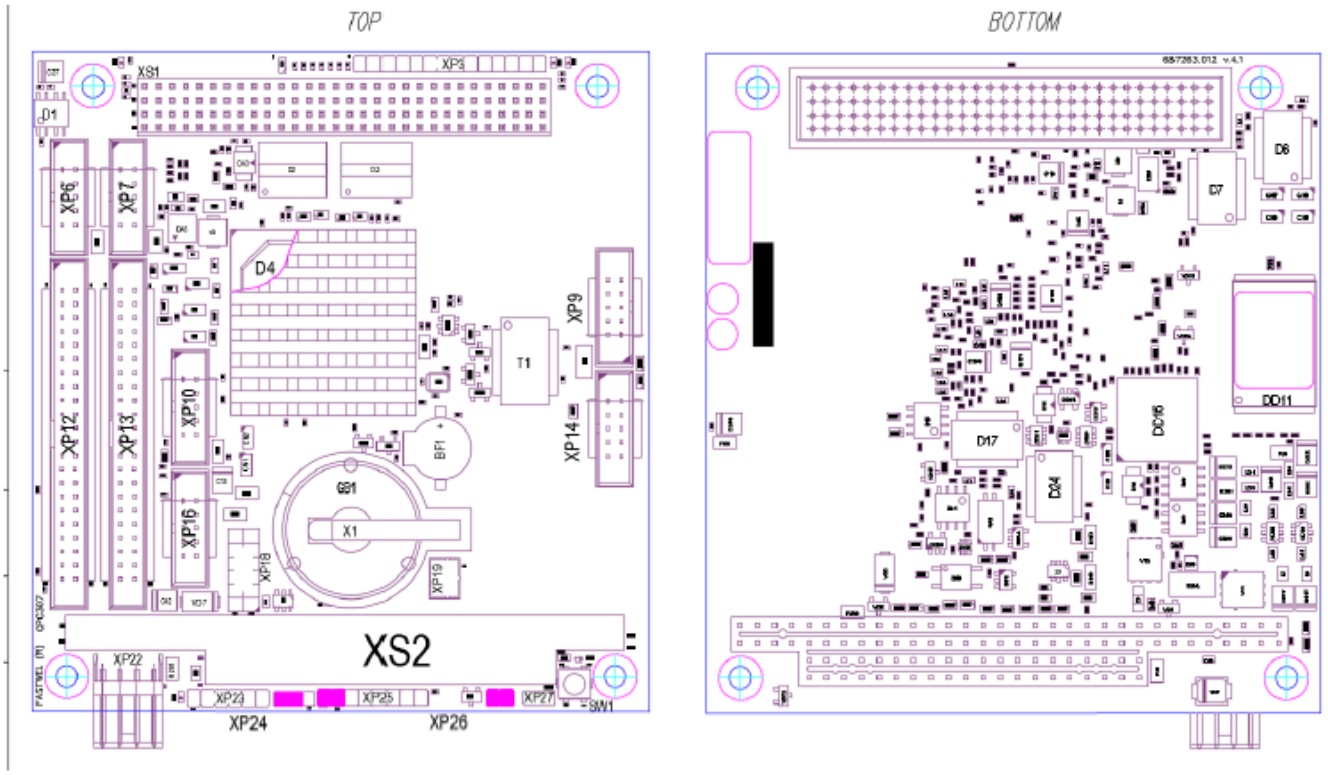


Figure 4.5 b) Location of connectors and main components on the TOP and BOTTOM sides for the CPC307-03 version (valid for CPC307 v.4.x)

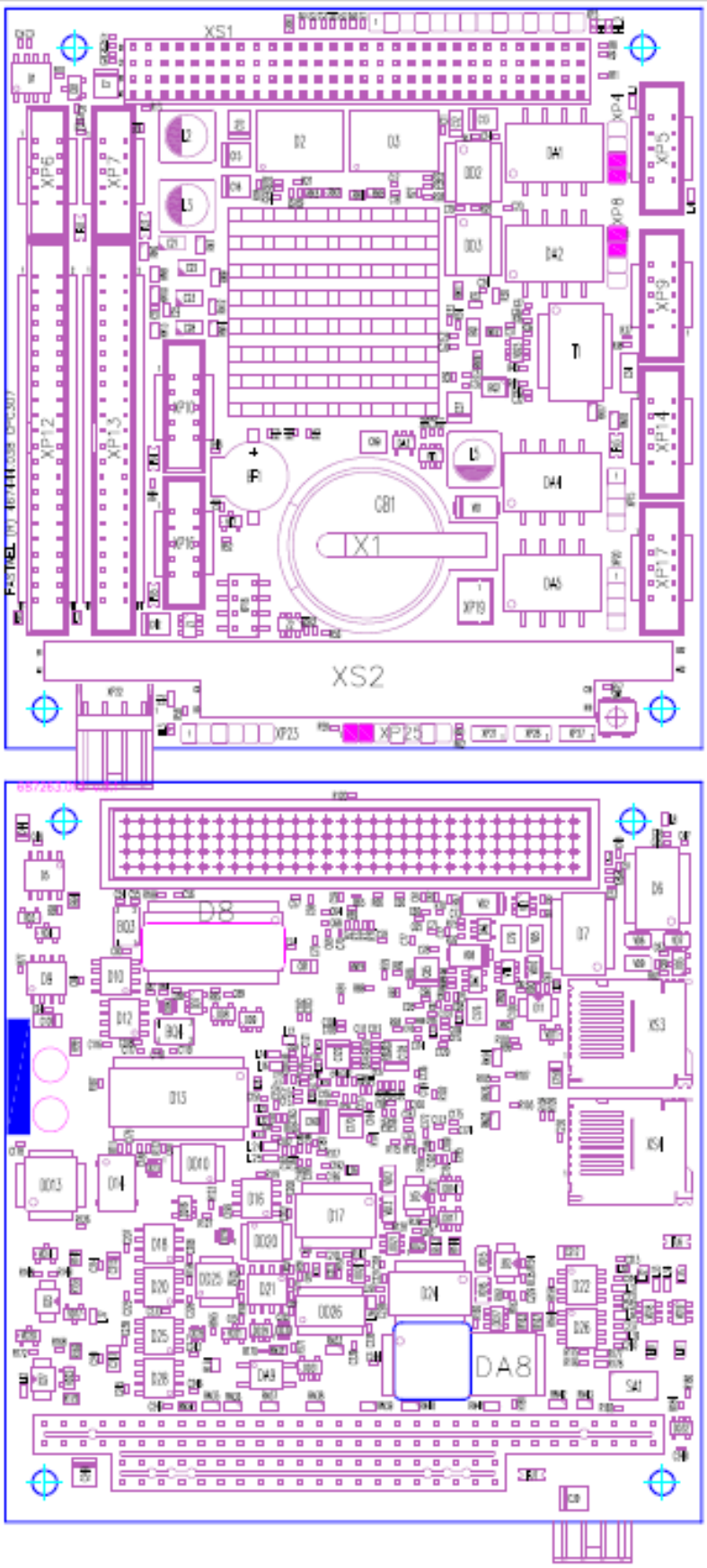


Figure 4.6 a) Location of connectors and main components on the TOP and BOTTOM for the CPC307-04 version (valid for CPC307 v.3.x)

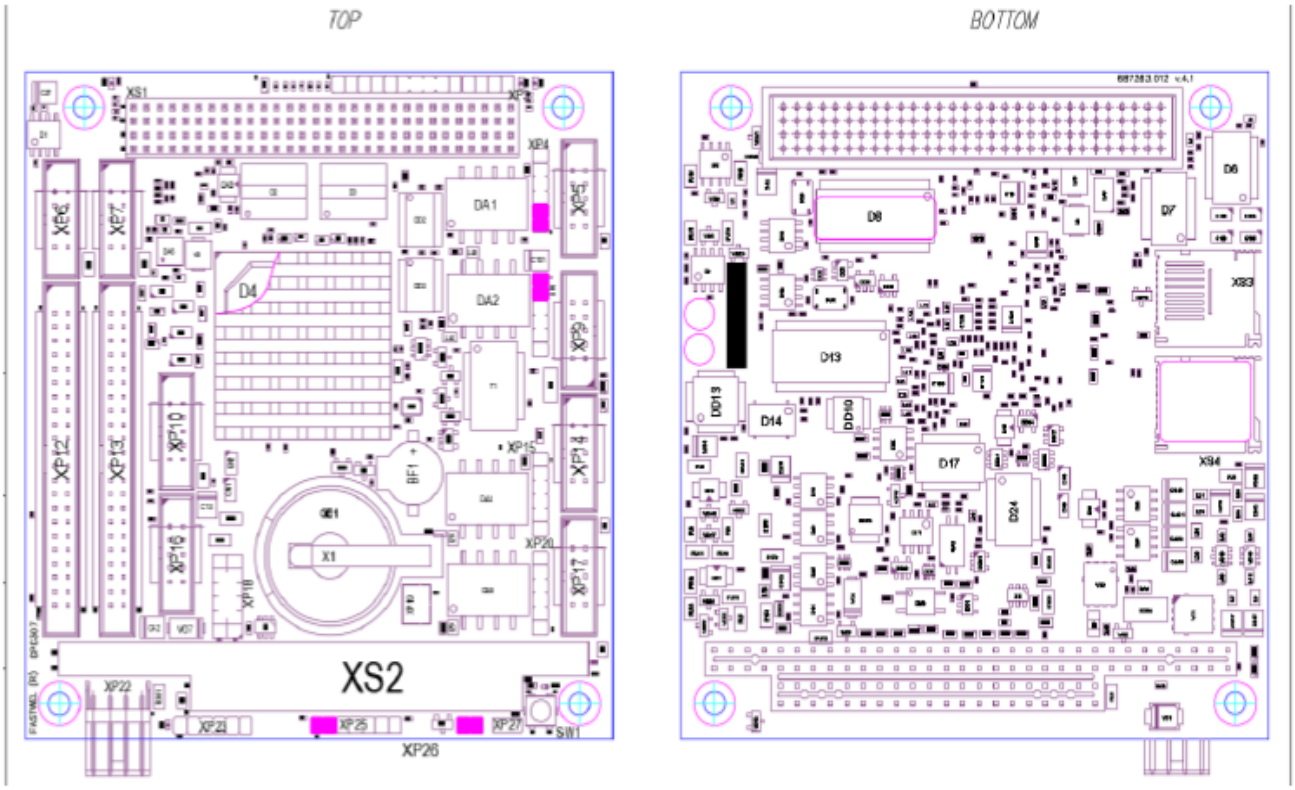


Figure 4.7 b) Location of connectors and main components on the TOP and BOTTOM sides for the CPC307-04 version (relevant for CPC307 v.4.x)

4.2 Address Space Allocation

4.2.1 Address space allocation

Table 4.1. Address space allocation of the first megabyte of memory

Range of addresses	Size	Description
00000h – 9FFFFh	640 KB	RAM
A0000h – BFFFFh	128 KB	PCI/ISA VGA Graphics
C0000h – C7FFFh	32 KB	VGA BIOS
C8000h – CFFFFh	32 KB	Expansion Card Boot ROM
D0000h - EFFFFh	128 KB	Not USED
F0000h – FFFFFh	64 KB	BIOS

4.2.2 I/O address space allocation

Table 4.2. I/O address space allocation

Range of addresses	Function	Note
0000h – 001Fh	8237 DMA Controller #1	–
0020h – 0021h	8259 Master Interrupt Controller	–
0022h – 0023h	Indirect Access	WDT0
0024h – 002Dh	ISA bus	Access to external bus
002Eh – 002Fh	Reserved	Not available
0030h – 003Fh	ISA bus	Access to external bus
0040h – 0043h	8253 Programmable Timer	–
0044h – 0047h	ISA bus	Access to external bus
0048h – 004Bh	Reserved	Not available
004Eh – 005Fh	ISA bus	Access to external bus
0060h – 0064h	8042 Keyboard Controller	–
0065h	WDT0	–
0066h	ISA bus	Access to external bus
0067h – 006Dh	WDT1	–
006Eh – 006Fh	ISA bus	Access to external bus
0070h – 007Fh	RTC, NMI Mask Register	–
0080h – 009Fh	DMA Page Registers	–
00A0h – 00B1h	8259 Slave Interrupt Controller	–

00B2h – 00BFh	ISA bus	Access to external bus
00C0h – 00DFh	8237 DMA Controller #2	–
00E0h – 01EFh	ISA bus	Access to external bus
01F0h – 01F8h	Primary IDE Controller	–
01F9h – 0277h	ISA bus	Access to external bus
0278h – 027Fh	LPT port	(possible assignment)
0280h – 02E7h	ISA bus	Access to external bus
Range of addresses	**Function**	**Note**
02E8h – 02EFh	Serial Port 4	(possible assignment)
02F0h – 02F7h	ISA bus	Access to external bus
02F8h – 02FFh	Serial Port 2	(possible assignment)
0300h – 0377h	ISA bus	Access to external bus
0378h – 037Fh	LPT port	(possible assignment)
0380h – 03AFh	ISA bus	Access to external bus
03B0h – 03BBh	MDA Adapter	(possible assignment)
03BCh – 03BFh	LPT port	(possible assignment)
03C0h – 03CFh	EGA, VGA Adapter	(possible assignment)
03D0h – 03DFh	CGA Adapter	(possible assignment)
03E0h – 03E7h	ISA bus	Access to external bus
03E8h – 03EFh	Serial Port 3	(possible assignment)
03F0h – 03F7h	Floppy Controller #1	(possible assignment)
03F8h – 03FFh	Serial Port 1	(possible assignment)
0400h – 04CFh	ISA bus	Access to external bus
04D0h – 04D1h	Reserved	Not available
04D2h – 0777h	ISA bus	Access to external bus
0778h – 077Fh	Reserved	Not available
0780h – 0CF7h	ISA bus	Access to external bus
0CF8h – 0CFFh	Configuration registers of the host PCI controller	–
0D00h – EDFFh	ISA bus	Access to external bus
EE00h – EF3Fh	Reserved	Not available
EF40h – FBFFh	ISA bus	Access to external bus
FC00h – FC0Dh	Reserved	Not available
FC0Eh – FFEFh	ISA bus	Access to external bus
FFF0h – FFFFh	Reserved	Not available

4.2.3 Integrated address decoder

The module has two CAN controllers, the SJA1000T and a controller for two RS-232 serial ports, the XR16C2850IM. These controllers must be assigned with base addresses and address space ranges prior to their use.

To address these controllers, the Vortex86DX SoC integrated address decoders are used - the GPCS0, GPCS1 (General Purpose Chip Select) lines. For their work each decoder must specify a base address, which starts the decoding, and the range of addresses to be covered - the mask of the base address. These register addresses are located in the I/O area of PCI devices and are accessible via the PCI configuration registers (CF8h and CFCh).

The GPCS0 base address is Bus 0, Device 7, Function 0, register 90h

GPCS0 address mask - Bus 0, Device 7, Function 0, register 94h

GPCS1 base address - Bus 0, Device 7, Function 0, register 98h

GPCS1 address mask - Bus 0, Device 7, Function 0, register 9Ch

The structure of registers GPCS0, GPCS1 is shown in Table 4.3.

Table 4.3. Structure of GPCS0 and GPCS1 registers

Bit	Name	Attribute	Description
Chip Select 0 Base Address Register			
31-1	BA	R/W	Base address, [31-0] for the memory address range, [15-1] for the range of I/O addresses
0	EN	R/W	Address decoding authorization
Chip Select 0 Base Address Mask			
31-28	Reserved	RO	Reserved
27	RD	R/W	Decoding enabled for read operations on the ISA bus (IOR#, MEMR#)
26	WR	R/W	Decoding enabled for write operations on the ISA bus (IOW#, MEMW#)
25	B16	R/W	0 – 8 bit (sampling is active for 8-bit operations) 1 – 16 bit (sampling is active for 16-bit operations)
24	MIO	R/W	0 – decoding during I/O operations 1 – memory address range decoding
23-1	BAM	R/W	Address mask, [31-9] for memory address range (MIO=1), [15-1] for I/O operations (MIO-0)
0	Reserved	RO	Reserved
Chip Select 1 Base Address Register			

31-1	BA	R/W	Base address, [31-0] for the memory address range, [15-1] for I/O address range
0	EN	R/W	Address decoding authorization
Chip Select 1 Base Address Mask			
31-28	Reserved	RO	Reserved
27	RD	R/W	Enable decoding for read operations on the ISA bus (IOR#, MEMR#)
26	WR	R/W	Enable decoding for write operations on the ISA bus (IOW#, MEMW#)
25	B16	R/W	0– 8 bit (sampling is active for 8-bit operations) 1– 16 bit (sampling is active for 16-bit operations)
24	MIO	R/W	0 – decoding during I/O operations 1 – memory address range decoding
23-1	BAM	R/W	Address mask, [31-9] for memory address range (MIO=1), [15-1] for I/O operations (MIO-0)
0	Reserved	RO	Reserved

4.2.3.1 Address space of CAN1, CAN2 ports

The memory address range for accessing the CAN controllers can be assigned arbitrarily in the least significant megabyte area. The addresses of the controllers must follow one after the other subsequently - first CAN1, then CAN2. Each controller is assigned with a 256-byte memory range for addressing the controller registers and the next 256-byte memory range for resetting the controller.

In order to assign a range of addresses to the CAN controllers, you must specify the base address (BA) and the base address mask in the registers of the SoC Vortex86DX. You can change the preset base address in the BIOS Setup menu or programmatically via the PCI configuration registers.

Example of setting the base address through the PCI configuration registers.

Base address (BA) – 0xDF000,
- CAN1 – register area 0xDF000 – 0xDF0FF,
- CAN1 – controller reset 0xDF100 – 0xDF1FF (any write or read will reset the controller),
- CAN2 – register area 0xDF200 – 0xDF2FF,
- CAN2 – controller reset 0xDF300 – 0xDF3FF (any write or read will reset the controller).

Example of setting register values:
- write the address of the base address register 80003890 to port 0CF8;
- write the base address register value 0DF001 to the port 0CFC;
- write the address of the register of the base address mask 80003894 to the port 0CF8;

- write the value 0DFFFFFC of the register of the base address mask to the port 0CFC.

For CAN controllers on the module interrupts IRQ10 (CAN1) and IRQ11 (CAN2) are hardware set. The preset address values are specified in Table 4.4.

Table 4.4. Preset address value for CAN1 and CAN2 interfaces

	CAN1	CAN2
Control area	DF000 – DF0FF	DF200 – DF2FF
Reset area (when accessing these addresses the corresponding CAN controller is reset)	DF100 – DF1FF	DF300 – DF3FF
ISA bus interrupt line	IRQ10	IRQ11

4.2.3.2 Address space of COM5, COM6 ports

The memory address range for accessing the serial ports COM5, COM6 can be assigned arbitrarily in the I/O port area. The addresses must follow one after the other subsequently - first COM5, then COM6. Each port is assigned 8 bytes of address in the I/O area.
In order to assign a range of COM5, COM6 port addresses, you must specify a base address (BA) and a base address mask in the Vortex86DX SoC registers. You can change the preset base address in the BIOS Setup menu or programmatically via the PCI configuration registers.

Example of setting the base address through the PCI configuration registers.

Base address – 220,
- COM5 – registers area 220 – 227,
- COM6 – registers area 228 – 22F.

Example of setting register values:
- write the address of the base address register 80003898 to port 0CF8;
- write the value of the base address register 221 to the port 0CFC;
- write the address of the base address mask register 8000389C to the port 0CF8;
- write the value of 0C00FFF0 of the base address mask register to the port 0CFC.

For controllers COM5 and COM6, the interrupts IRQ7 (COM5) and IRQ9 (COM6) are hardware set on the module. Preset addresses for COM5, COM6 ports are shown in Table 4.5.

Table 4.5. Preset address values for COM5 and COM6 ports

	COM5	COM6
Control area	220 – 227	228 – 22F
ISA bus interrupt line	IRQ7	IRQ9

4.2.4 Distribution of interrupt lines

By default, interrupt requests are generated by devices included in the module. The interrupt sources are shown in Table 4.6. Interrupt requests configuration is set in the BIOS Setup menu.

Table 4.6. Distribution of interrupt lines in the CPC307 module

Nodes that use interrupt lines		NMI	Number of IRQ interrupt line														
			0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
System timer			•															
PS/2 keyboard				•														
PS/2 mouse															•			
Cascading					•													
COM 1						○	•					○	○	○				
COM 2						•	○					○	○	○				
COM 3						○	•					○	○	○				
COM 4						•	○					○	○	○				
COM 5										•								
COM 6												•						
CAN 1													•					
CAN 2														•				
LPT								•		○								
RTC											•							
Ethernet																		•
USB										•		•	•	•				
Co-Processor																•		
IDE (Primary Channel)																	•	
WDT0		○				○	○	○	○	○		○	○	○	○		○	○
WDT1		○				○	○	○	○	○		○	○	○	○		○	○
WDT2		o				○	○	○	○	○		○	○	○	○		○	○
External Isolated Interrupt		o				○	○	○	○	○		○	○	○	○		○	○
PC-104		o				○	○	○	○	○		○	○	○	○		○	○
PCI-104	INT A					○	○	○	○	○		○	○	○	○		○	○
	INT B					○	○	○	○	○		○	○	○	○		○	○
	INT C					○	○	○	○	○		○	○	○	○		○	○
	INT D					○	○	○	○	○		○	○	○	○		○	○

The conventional symbols used in Table 4.6:

	Switching is not allowed
○	Switching is allowed
•	Switching is set by default
o	Switching is done via the IOCHK# signal of the ISA bus.

The allocation of hardware interrupts can only be changed using the BIOS.
The IRQ[3...7], IRQ[9...12], IRQ[14...15] interrupt lines are hardware connected to the PC/104 connector on the board.

4.2.5 Distribution of direct memory access channels

Table 4.7. Distribution of direct memory access channels

	LPT - port	PC/104 Connector (ISA)
DREQ0	•	
DREQ1	○	•
DREQ2	○	•
DREQ3	○	•
DREQ5		•
DREQ6		•
DREQ7		•

Conventional symbols used in Table 4.7:

	Switching is not allowed
○	Switching is allowed
•	Switching is set by default

The allocation of DMA requests can only be changed using the BIOS.
The DREQ[0..3], DREQ[5..7] lines are hardware connected to the PC/104 connector on the board.

4.3 Description of the main functional elements of the module

4.3.1 Vortex86DX SoC

DM&P Vortex86DX SoC includes:

- 32-bit x86 processor core operating at 600 MHz;
- L1 cache of 32 KB;
- L2 cache of 256 KB;
- math coprocessor;
- 16-bit DDR2 SDRAM memory bus;
- IDE controller (combined with the SD interface controller);
- 5 x RS-232 serial ports;
- universal parallel port;
- 4 x USB 2.0 ports;
- PS/2 keyboard and mouse connection port;
- PCI bus controller;
- ISA bus controller;
- LPC bus controller;
- SPI bus controller;
- two I2C interfaces;
- integrated Ethernet 10/100 controller;

- real-time clock;
- CMOS memory for storing settings;
- In-built Flash memory for BIOS storage;
- two programmable watchdog timers.

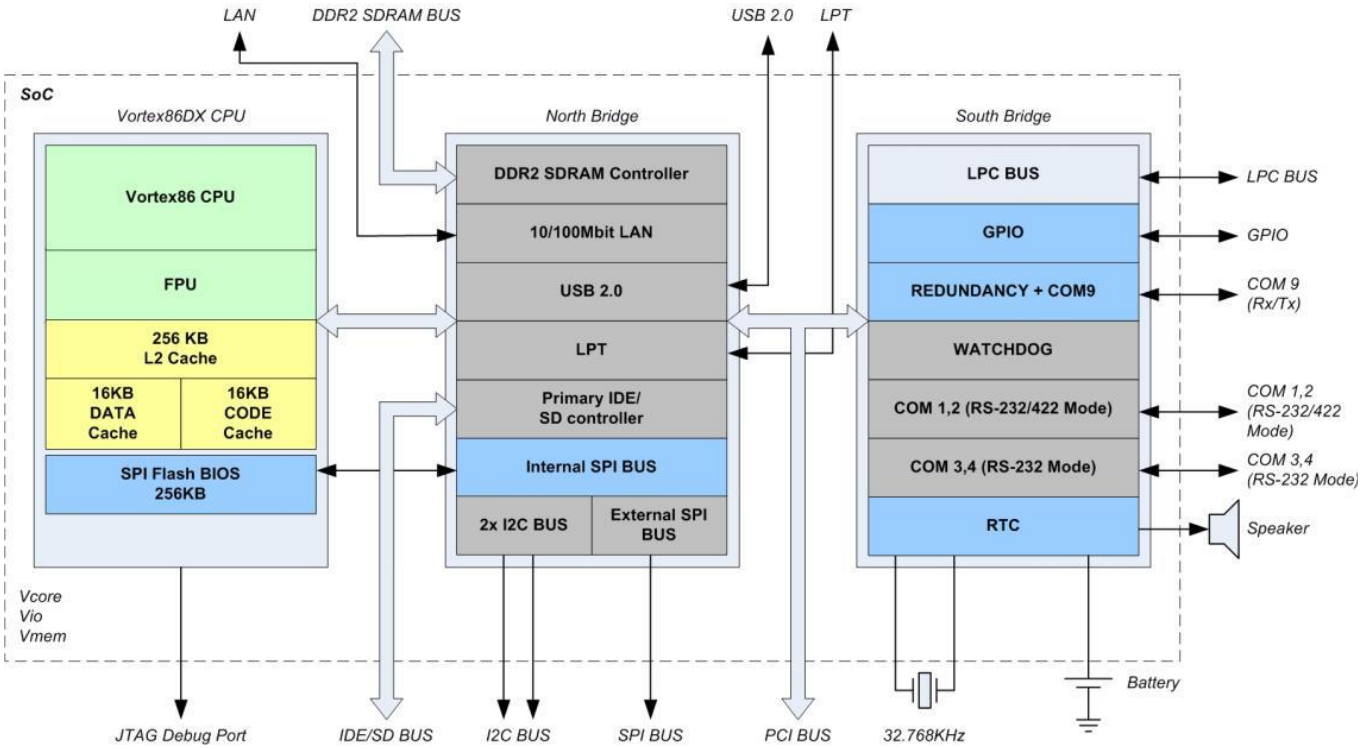


Figure 4. 8.Block diagram of Vortex86DX SoC

4.3.2 DDR2 Memory

Two DDR2 SDRAM chips with a total size of 256 Mbytes are soldered on the module, working at 266 MHz (for module versions older than 4.x) or 333 MHz (for module versions 4.x). Installation of memory expansion modules is not provided. The maximum possible memory size is 256 Mbytes.

4.3.3 IDE interface

Two external IDE devices, such as HDD, Compact Flash adapter, etc., can be connected to the module. Connection is carried out to the XP13 connector where the Primary IDE interface is routed. UDMA2 mode is supported.
The CPC307-04 version is capable of connecting two microSD memory cards; see paragraph 4.3.4 MicroSD for a detailed description.
If the soldered ATA Flash Disk controller is enabled, one additional external IDE-device can be connected to the module (Table 4.8).
If the soldered ATA Flash Disk controller is prohibited, two additional external IDE devices can be connected to the module (par. 4.3.5 ATA Flash disk controller, par. 4.3.20 Configuration jumpers).

Table 4.8. Possible configurations for connecting IDE devices to the module

ATA Flash Disk controller	XP13 (Primary IDE)	XS3, XS4 (microSD 1,2)
Enabled	Connection of one device	**No connection**
Disabled	Connection of two devices	**No connection**
Lacks (version CPC307-04)	Connection of two devices	**No connection**
	No connection	Connection of two devices

For the CPC307-04 module make sure that no microSD cards are connected to the module and the "Parallel IDE" mode is selected in the BIOS Setup menu for the Primary IDE port (paragraph 5.2.2 IDE Configuration).

Attention!

Simultaneous connection of IDE devices and microSD cards is NOT allowed.

The interface is routed to the XP13 connector (IDC2-44, a 2-way male connector).
Pin assignment of the XP13 connector is shown in Table 4.9.
The module has a Leotronics 2073-3442 connector.
The recommended mating part is Leotronics 2040-3442 (ribbon cable press-on socket) or Leotronics 2022-2442 (socket) and 2023-2000 set of contacts.

Attention!

When connecting Compact Flash modules to the IDE port (XP13) using IDE - Compact Flash adapters, only Compact Flash modules that support UDMA-5 mode or higher may be used. Use of other Compact Flash cards can cause the CPC307 module to fail (integrated Flash Disk) and will not be covered by the warranty (due to different voltage levels on the IDE signal lines for different Compact Flash modules).

Table 4.9. Pin assignment of the XP13 for connection of IDE devices

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	RESET#	2	GND	23	IOWR#	24	GND
3	DD7	4	DD8	25	IORD#	26	GND
5	DD6	6	DD9	27	IORDY	28	GND
7	DD5	8	DD10	29	DACK#	30	GND

9	DD4	10	DD11	31	IRQ	32	IOCS16#
11	DD3	12	DD12	33	A1	34	PDIAG#
13	DD2	14	DD13	35	A0	36	A2
15	DD1	16	DD14	37	CS0#	38	CS1#
17	DD0	18	DD15	39	DASP#	40	GND
19	GND	20	–	41	+5 B	42	+5 B
21	DRQ	22	GND	43	GND	44	–

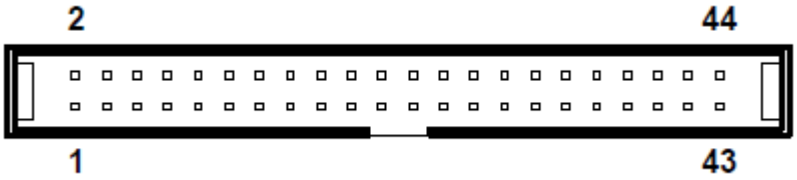


Figure 4.9 Numbering of the XP13 connector pins

The 2½" HDD connects directly to the XP13 using the ACS00010 cable (FC44). Other types of HDD (3½" format), as well as CDROMs having a 40-pin connector with 2.54 mm pitch, are connected to the module through the CDM02 adapter module (FAPI.469535.023). The adapter plugs directly into a 40-pin HDD or CDROM socket and connects to the XP13 with an ACS00010 (FC44) cable.
Operation modes of external IDE devices are set by configuring appropriate jumper(s) on external IDE devices.

Table 4.10 shows the recommended configurations for IDE devices.

Table 4.10.Recommended configurations for IDE devices

master \ slave	ATA Flash disk NAND controller	Compact Flash	SSD	HDD	DVD-ROM
ATA Flash disk NAND controller		+	+	+	+
Compact Flash	+ [1]		+	+	+ [2]
SSD	+	-		+	+
HDD	+	+	+		+
DVD-ROM	+	+ [2]	+	+	

1 – to identify the onboard NAND-flash drive after power-up you need to RESET the module (SW1 or the corresponding key combination on the keyboard);
2 - The DVD drive must be connected strictly to the far end of the IDE ribbon cable connector.

4.3.4 MicroSD

Two microSD cards can be connected to the CPC307-04 version. Connection is made to the XS3 and XS4, which are connected to the SD interface. These connectors are for microSD and microSDHC memory cards only.
Make sure that no IDE devices are connected to the module, and the "SD Card" mode is selected in the BIOS Setup menu for the Primary IDE port.

Attention!
Simultaneous connection of IDE devices and microSD memory cards is NOT allowed.

The interface is routed to the XS3 (Channel 0) and XS4 (Channel 1) connectors.
The pin assignment of the XS3 and XS4 connectors is given in Table 4.11.
The module is equipped with Hirose DM3B-DSF-PEJ connectors.

Table 4.11. Pin assignment of XS3 and XS4 for connection of microSD cards

Pin	Signal	Pin	Signal
1	DAT2	6	GND
2	CD/DAT3	7	DAT0
3	CMD	8	DAT1
4	VCC (+3.3V)	9	CDSwA
5	CLK	10	CDSwB (GND)

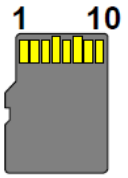


Figure 4.10. Numbering pins of the microSD memory card

4.3.5 ATA Flash disk controller

The module has a NAND Flash memory controller chip (ATA Flash disk controller), which is connected to the Primary IDE interface. A 1 GB (for versions older than 4.x) or 2 GB (for 4.x versions) Flash memory chip, using NAND technology, is connected to this controller. This controller is detected by the system as an IDE drive and can be used as a boot drive.
With a jumper placed on pins 1-2 of the XP24 connector, the controller is in master mode on the IDE bus. If the jumper is removed, it is in “slave” mode.
The controller can be forcibly disabled by setting the jumpers 2-3 contacts of the XP24 connector (paragraph 4.3.20 Configuration jumpers) - the above information is only relevant for versions 4.x, limitations specified in Section 8 apply to versions 3.x.

Note
The maximum reading speed can be about 13.5 MB/s, and the maximum writing speed is 7.5 MB/s.

4.3.6 PS/2-keyboard and mouse

A keyboard and/or mouse with PS/2 interfaces can be connected to the module. This interface is routed to the XP23 6-pin connector.
The interface is routed to the XP23 connector (IDC2-6, single-row, 2 mm male connector).
Pin assignment of the XP23 connector is specified in the Table 4.12.
The module has a PLS2-40/6 connector.
The recommended mating part is Leotronics 2018-3061 (socket) and 2023-2000 set of contacts.

Table 4.12. Pin assignment of XP23 connector for PS/2 keyboard and mouse connection

Pin	Signal	Pin	Signal
1	KBD CLK	4	GND
2	KBD DATA	5	+5 B
3	MOUSE CLK	6	MOUSE DATA

Figure 4.11. Numbering pins of the XP23 connector

4.3.7 Opto-isolated reset/interrupt

The module has an XP19 connector, which can be used to generate an opto-isolated remote reset or interrupt signal, depending on the XP25 connector jumper setting. This signal can be switched as follows:
- module reset (with a jumper installed on pins 1-2 of the XP25 connector);
- GPIO1 line 0 (when the jumper is installed to contacts 4-5 of the XP25 connector). You can set the reset function or IRQx interrupt number to be generated by an external opto-isolated signal in the BIOS Setup menu or by programming the GPIO1 port registers;
- NMI interrupt generation (with the jumper on pins 5-6 of the XP25 connector installed). In such a configuration, the external opto-isolated input signal is switched to the IOCHK# line of the ISA bus.

The XP25 connector also sets the function of the PFO# (Power Fail Output) signal of the external power supply supervisor chip (paragraph 4.3.18 Module Power Supply Supervisor). The PFO# signal is set to “0” when the input voltage of +5V falls down to +4.45V. The following switching of the PFO# signal is possible:
- Module reset at active PFO# signal level (with jumper installed on pins 2-3 of XP25 connector);
- Line 0 port GPIO1 (with the jumper installed on contacts 3-4 of the XP25 connector). You can set the reset function or IRQx interrupt number to be generated by the PFO# signal in the BIOS Setup menu or by programming the GPIO1 port registers;

- NMI interrupt generation (with the jumper installed on pins 5-6 of the XP25 connector). With such a configuration, the PFO# signal is switched to the IOCHK# line of the ISA bus.

See also paragraph 4.3.20 Configuration jumpers, paragraph 4.3.19 GPIO ports.

The PFO# signal is described in more detail in paragraph 4.3.18 Module power supply voltage supervisor.

Figure 4.12 shows the implementation diagram of the opto-isolated reset/shutdown.

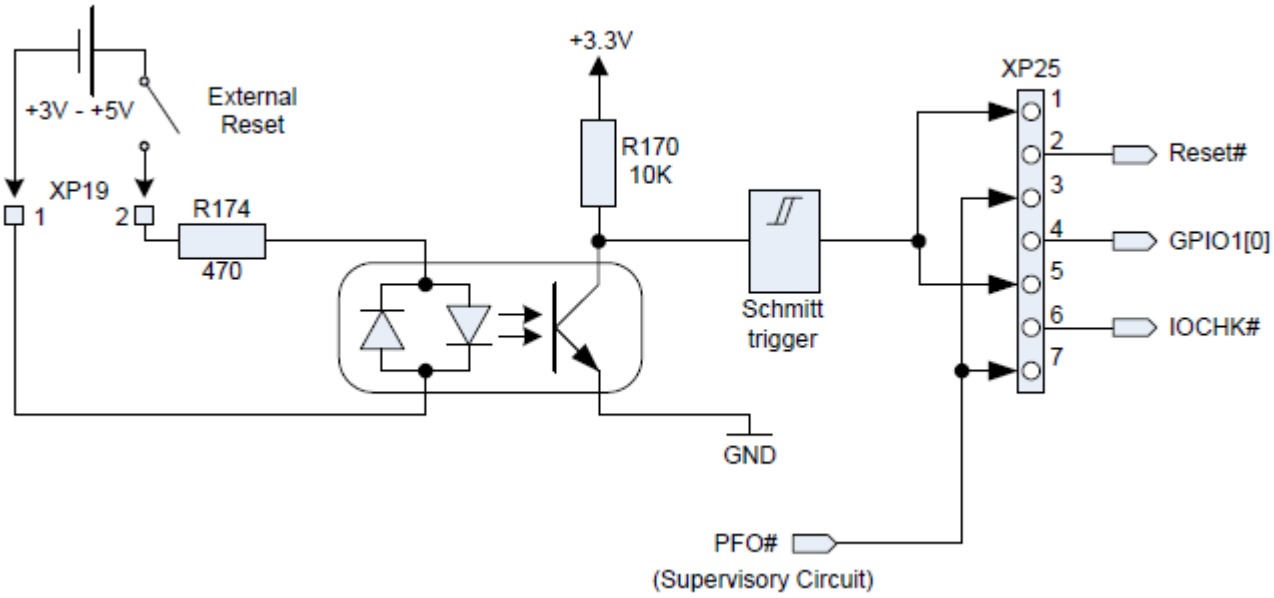


Figure 4.12. Reset source selection and switching diagram of the opto-isolated input

The external reset/interrupt circuit is connected to the XP19 connector. The location of the first pin of this connector on the module is shown in Figure 4.13.

The module has a JST B 2B-PH-KL connector.

The recommended mating part is the JST PHR-2 and SPH-002T-P0.5S set of contacts.

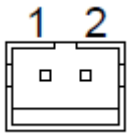


Figure 4.13. Numbering pins of the XP19 connector

4.3.8 USB interface

Up to 4 x USB devices can be connected to the module. The interfaces are routed to the part of the XP12 connector pins.

The module has 4 x USB-host ports. USB 1.1 (High-Speed) and USB 2.0 (Full-Speed) specifications are supported. The mode of interfaces operation is set in the BIOS Setup menu.

Each channel has power protection (+5V, 500mA).

Booting from USB ports is supported, emulation (operation) mode and boot sequence are set in the BIOS Setup menu. Depending on the type and manufacturer of USB devices you may need to change the emulation mode and type or the system may be completely incompatible. Each specific USB device requires a separate compatibility check to ensure stable operation.

By default, 512MB or less USB-Flash devices are detected by the system as FDD (Floppy Disk Drive) and are assigned with A, B letters. No more than two FDDs are supported on the system.

All four channels are routed to the part of the XP12 connector pins (IDC2-44, two-row male connector with 2 mm pitch).

XP12 connector pin assignments relevant to USB interfaces are given in Table 4.13.

A Leotronics 2073-3442 connector is installed on the module.

The recommended mating part is Leotronics 2040-3442 (ribbon cable press-on socket) or Leotronics 2022-2202 (socket) and 2023-2000 set of contacts.

Table 4.13. Pin assignment of the XP12 for connection of USB devices

Pin	Signal	Pin	Signal
27	+5 V (USB1)	28	+5 V (USB2)
29	D1-	30	D2-
31	D1+	32	D2+
33	GND (USB1)	34	GND (USB2)
35	–	36	–
37	+5 V (USB3)	38	+5 V (USB4)
39	D3-	40	D4-
41	D3+	42	D4+
43	GND (USB3)	44	GND (USB4)

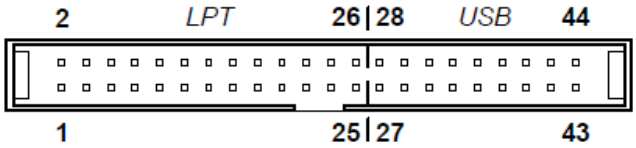


Figure 4.14. Numbering pins of the XP12 connector

4.3.9 Ethernet-port

One Ethernet channel can be connected to the module. 10/100 Mbps speeds are supported.

The Ethernet controller is integrated into the Vortex86DX SoC.

The interface is routed to an XP9 connector (IDC2-10, two-row male connector with 2 mm pitch).

XP9 connector pin assignment is shown in Table 4.14.

A Leotronics 2073-3102 connector is installed on the module.

The recommended mating part is 2039-3101 (ribbon cable press-on socket) or Leotronics 2022-2102 (socket) and 2023-2000 set of contacts.

Attention!
At ambient temperatures below 0 ºC, the real exchange rate of the Ethernet port may decrease. For example, at ambient temperature of -30 ºC and below the real exchange speed may decrease to 10 Mbit/sec even if the mode is set to 100 Mbit/sec.
To solve this problem you need to update your BIOS to version 3.25 or newer (BIOS release date should be 04.12.2017 or later).

Table 4.14. Pin assignment of the XP9 connector of Ethernet-port

Pin	Signal	Pin	Signal
1	TX1+ (Ethernet1)	2	TX1- (Ethernet1)
3	RX1+ (Ethernet1)	4	RX1- (Ethernet1)
5	–	6	–
7	–	8	–
9	–	10	–

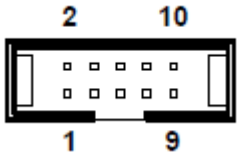


Figure 4.15. Numbering pins of the XP9 connector

4.3.10 Serial ports

4.3.10.1 COM1 and COM2

COM1 and COM2 ports operate in RS-232 or RS-485/422 interface mode and have standard PC/AT base addresses. The interrupt line and base address for the serial ports are selected in the BIOS Setup menu.
The mode of each port is set in the BIOS Setup menu or by controlling the GPIO2 port (paragraph 4.3.19 GPIO Ports). The default operating mode for COM1 and COM2 is RS-232.
The maximum baud rate for COM1 and COM2 ports is 115.2 kbaud. The ports are fully software compatible with the UART 16550 model.
The transmitters in the RS-422/485 mode are hardware controlled. The mode of operation of each port is selected independently of the other.
When using the COM1 and COM2 serial ports, the maximum number of connected devices is limited: 16.

RS-232 Operation Mode

In RS-232 mode the ports operate as a full-fledged 9-wire interface.
For COM1 port, the RS-232 mode is set by shifting GPIO2 port line 0 to “1” and setting the line direction to "out".

For COM2, the RS-232 mode is set by shifting GPIO2 port line 2 to “1” and setting the direction of the line to “output”.

RS-422/485 operation mode

In RS-422/485 mode the ports work with hardware control of the transmitter and with the receiver permanently on. In RS-485 mode (half duplex RS-485/422 converter mode) the TX+ and RX+ lines are closed in the driver, as well as TX- and RX- lines from the interface connector side (Figure 4.17). In RS-422 mode these lines are not closed and output to the connector separately, according to Table 4.15 and Table. 4.16.

For COM1 port, the RS-422/485 mode is set by shifting the GPIO2 port line 0 to “0” and setting the direction of the line to “output”.

For COM2 port, the RS-422/485 mode is set by shifting GPIO2 port line 2 to “0” and setting the direction of the line to “output” mode.

For COM1 port, Half-Duplex mode is set by shifting GPIO2 port line 1 to “1”. The Full-Duplex mode is set by shifting GPIO2 port line 1 to “0”. The direction of GPIO2 port line 1 must be set to “out” mode.

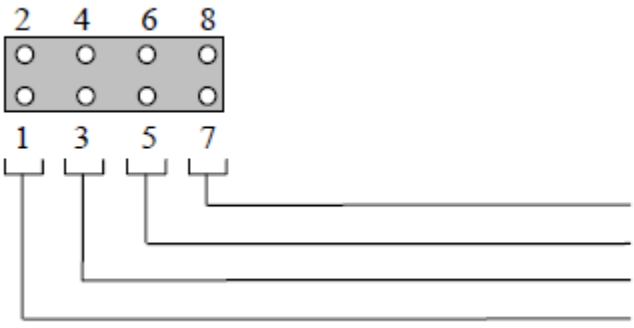
For COM2 port, the Half-Duplex mode is set by shifting GPIO2 port line 3 to “1”. The Full-Duplex mode is set by shifting GPIO2 port line 3 to “0”. The direction of GPIO2 port 3 line must be set to “out” mode.

The COM1 and COM2 ports have the possibility to connect terminators by setting appropriate jumpers on the XP18 connector. The rating of termination resistors is 120 ohms (± 5%). In the 4.x versions of the module using the XP18 connector you can set an offset of ±200 mV along the TX+ and TX- lines (for more details see paragraph 4.3.21).

In module versions 3.x and below:

- To connect the Rtr terminating resistor to the RX-/RX+ line a jumper should be installed to pins 3-4 of the XP18 connector for the COM1 port and/or to pins 7-8 of the XP18 connector for the COM2 port.

- To connect the Rtt terminating resistor to the TX-/TX+ line a jumper should be installed to pins 1-2 of the XP18 connector for the COM1 port and/or to pins 5-6 of the XP18 connector for the COM2 port (paragraph 4.3.20 Configuration jumpers).



XP18 - connection of terminating resistors for COM1, COM2 ports in RS-422/485 modes

Enabling Rtr for RX-/RX+ lines (COM2)
Enabling Rtt for TX-/TX+ lines (COM2)
Enabling Rtr for RX-/RX+ liens (COM1)
Enabling Rtt for TX-/TX+ lines (COM1)

Figure 4.16. Pin assignment of the XP18 connector (for module versions 3.x and lower)

When the RS-485 network state is inactive, all the drivers are set to the third state, hence all the nodes are in the receiving mode. Thus, the network state is not defined. If the potential difference at the RX+ and RX- inputs of the receiver is less than the threshold value of ±200 mV, then the logic level at the receiver output (RX) will be the value of the last received data bit. Safety bias

resistors are used to ensure proper voltage levels in the inactive state of the network. A 2.2 kΩ protective bias resistor (Rcm+) is installed to set the initial high level on the TX+ line. To set an initial low level on the TX- line, a 2.2 kOhm protective bias resistor (Rcm-) is installed (Figure 4. 17).

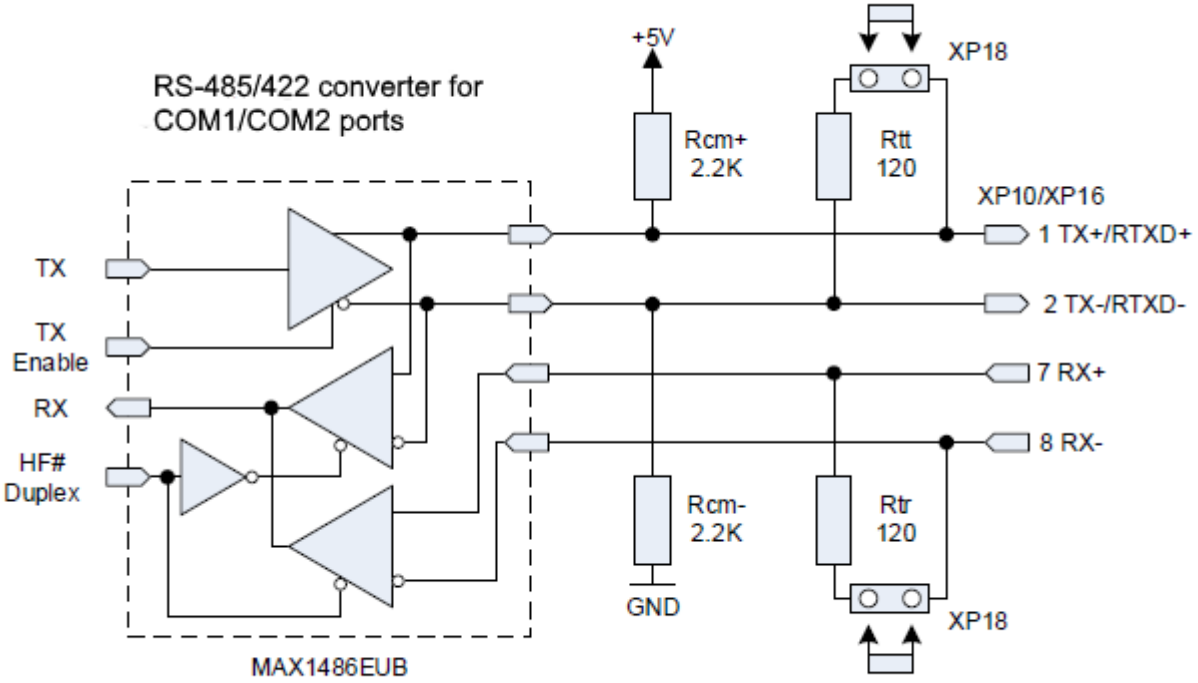


Figure 4.17. a) The RS-422/485 transmitter with bias elements and termination resistors (for module versions 3.x and lower)

In module versions 4.x and below:

The XP18 jumpers are used to connect the matching circuits to RS-422 or RS-485 interface signal lines and setting the operation mode.

To connect the Rtt terminating resistor to the TX-/TX+ line, set the following jumpers to pins 1-2 and 9-10 of the XP18 connector for COM1 port and/or to pins 5-6 and 11-12 of the XP18 connector for the COM2 port.

To connect the Rtr terminating resistor to the RX-/RX+ line, install a jumper to pins 3-4 of the XP18 connector for the COM1 port and/or to pins 7-8 of the XP18 connector for the COM2 port (paragraph 4.3.20 Configuration jumpers).

To generate a +200 mV offset on the Y/Z lines connect a 680 ohm resistor to supply voltage +5V of +TX signal by placing a jumper on pins 1-2 or 5-6 of the XP18 connector for COM1 or COM2 port, respectively.

To generate the -200 mV offset on the Y/Z lines, connect a 680 ohm resistor to the -TX of -TX signal by placing a jumper on pins 9-10 or 11-12 of the XP18 connector for COM1 or COM2, respectively.

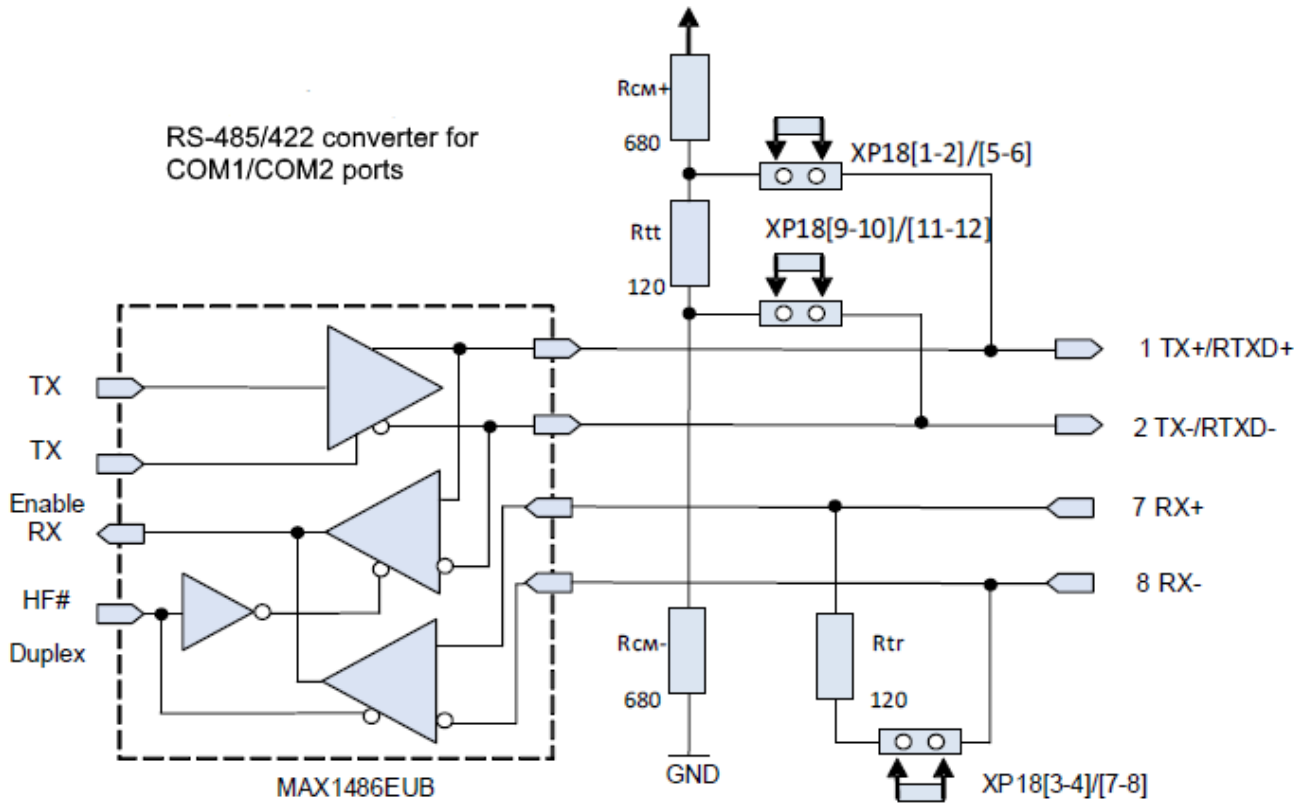


Figure 4.17. b) RS-422/485 transmitter with bias elements and with terminating resistors (for module 4x versions)

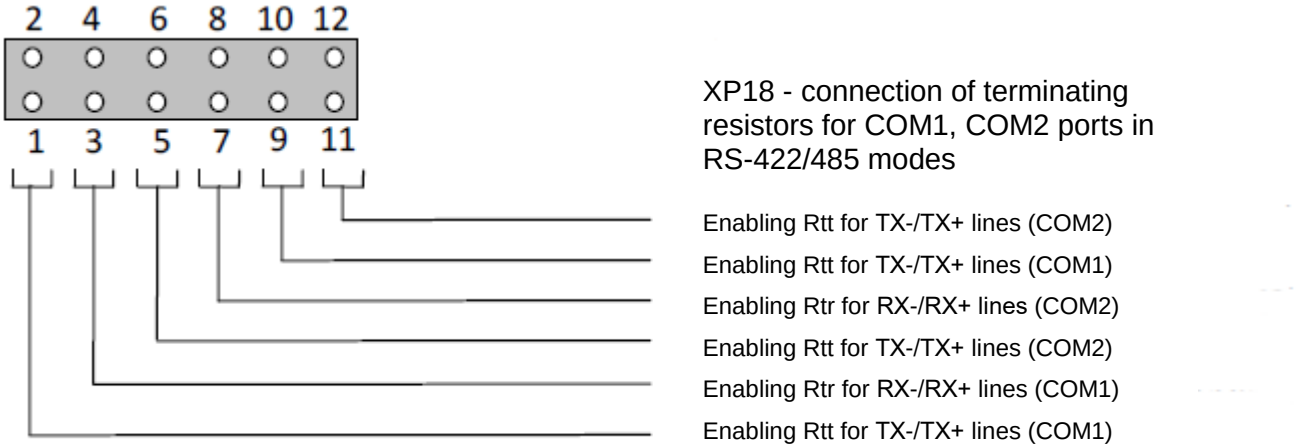


Figure 4.17. c) Pin assignment of the XP18 connector (for module versions 4.x and lower)

COM1 port is routed to the XP10 connector (IDC2-10, 2-row male connector with a pitch of 2 mm).
COM2 is routed to the XP16 connector (IDC2-10, 2-row male connector with a pitch of 2 mm).
Pin assignment of the XP10 connector is given in the Table 4.15.
Pin assignment of the XP16 connector is given in the Table 4.16.
2 x Leotronics 2073-3102 connectors are installed on the module.
The recommended mating part is Leotronics 2039-3101 (ribbon cable press-on socket) or Leotronics 2022-2102 (socket) and 2023-2000 set of contacts.
The maximum number of modules that can be connected to the RS-485 network together with the CPC307 module is 128, provided that the input impedance of the RS-485 drivers is minimum 96 kΩ. The maximum number of CPC307 modules combined within a single RS-485 network is no more than 16.

Attention!
A +5 V power supply circuit connects homonymous pins of XS1 (PCI-104), XS2 (PC-104), and XP22 (additional power connector) connectors and is intended for supplying the module with power. The +5 V power supply outputs are protected by a 0.5 A fuse. For connected external modules, the recommended current consumption value is not more than 0.4 A. It is not recommended to connect power from interface connectors to more than one external module in order not to overload the power supply circuits of the CPU module

Table 4.15. Pin assignment of the XP10 connector for COM1 port

Pin	Signal	Pin	Signal
1	DCD (RS-232)	2	DSR (RS-232)
	TX+/RTXD+ (RS-422/485)		TX-/RTXD- (RS-422/485)
3	RXD#	4	RTS
5	TXD#	6	CTS
7	DTR (RS-232)	8	RI (RS-232)
	RX+ (RS-422/485)		RX- (RS-422/485)
9	GND	10	+5 B

Table 4.16. Pin assignment of the XP16 connector for COM2 port

Pin	Signal	Pin	Signal
1	DCD (RS-232)	2	DSR (RS-232)
	TX+/RTXD+ (RS-422/485)		TX-/RTXD- (RS-422/485)
3	RXD#	4	RTS
5	TXD#	6	CTS
7	DTR (RS-232)	8	RI (RS-232)
	RX+ (RS-422/485)		RX- (RS-422/485)
9	GND	10	+5 B

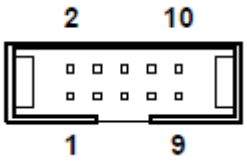


Figure 4.18. Numbering pins of the XP10 and XP16 connectors

Figure 4.19 shows the connection of modules via RS-422 interface.

Figure 4.20 shows connection of modules via RS-485 interface.

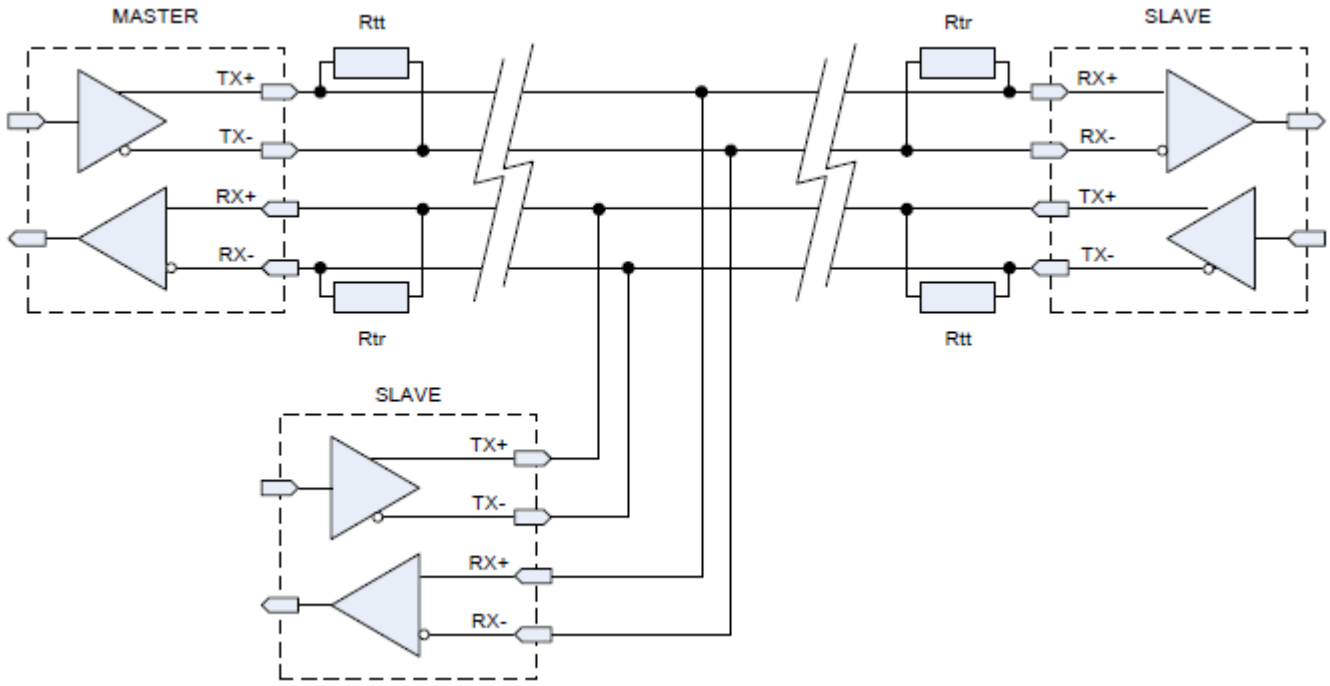


Figure 4.19. Connecting several devices via RS-422 Interface

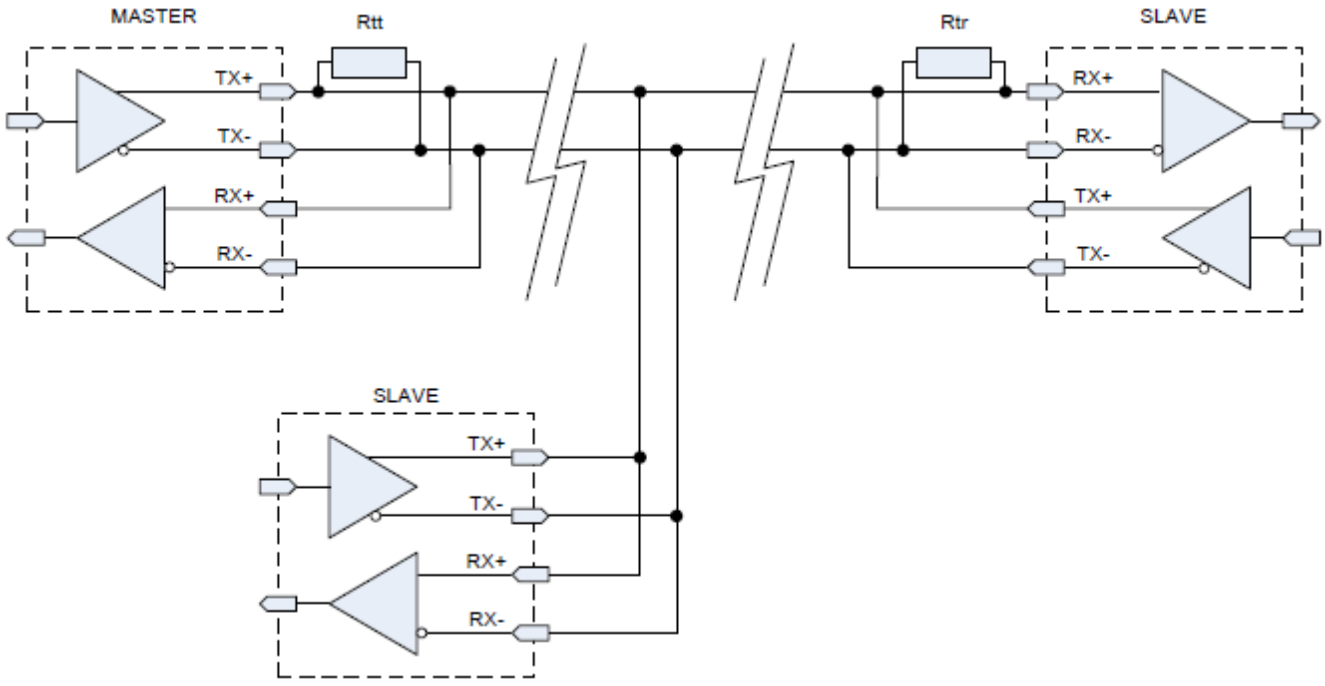


Figure 4.20. Connecting several devices via RS-485 interface

4.3.10.2 COM3 and COM4

COM3 and COM4 ports are working in 9-wire RS-232 interface mode and have standard base addresses for PC/CAT. Base addresses and interrupt lines for the serial ports are selected in the BIOS Setup menu.
The maximum baud rate for COM3 and COM4 ports is 115.2 kbaud. The ports are fully software compatible with the model UART 16550.
The COM3 port is routed to the XP6 conenctor (IDC2-10, 2-row male connector with a pitch of 2 mm).
The COM4 port is routed to the XP7 connector (IDC2-10, 2-row male connector with a pitch of 2 mm).
Pin assignment of the XP6 connector is shown in Table 4.17.
Pin assignment of the XP7 connector is shown in Table 4.18.
Two Leotronics 2073-3102 connectors are installed on the module.
The recommended mating part is Leotronics 2039-3101 (ribbon cable press-on socket) or Leotronics 2022-2102 (socket) and 2023-2000 set of contacts.

Attention!
+5 V power supply circuit connects homonymous pins of the XS1 (PCI-104), XS2 (PC-104) and XP22 (additional power connector) connectors and is designed for module's power supply. The +5 V power supply outputs are protected by a 0.5 A fuse. For connected external modules, the recommended current consumption value is not more than 0.4 A. It is not recommended to connect power from interface connectors to more than one external module in order not to overload the power supply circuits of the CPU module.

Table 4.17. Pin assignment of the XP6 connector for COM3 port

Pin	Signal	Pin	Signal
1	DCD	2	DSR
3	RXD#	4	RTS
5	TXD#	6	CTS
7	DTR	8	RI
9	GND	10	+5 B

Table 4.18. Pin assignment of the XP7 connector for COM4 port

Pin	Signal	Pin	Signal
1	DCD	2	DSR
3	RXD#	4	RTS
5	TXD#	6	CTS
7	DTR	8	RI
9	GND	10	+5 B

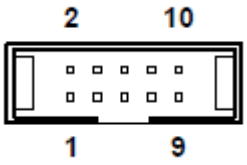


Figure 4. 21. Numbering pins of the XP6 and XP7 connectors

4.3.10.3 COM5 and COM6

COM5 and COM6 ports operate in the RS-422 interface mode. The base address (BA) for the serial ports is selected by programming the registers of the Vortex86DX SoC. Interrupt lines are set by the hardware. For more details see paragraph 4.2.3 Integrated address decoder.
Table 4.19 shows the resources assigned for each controller.

Table 4.19. Resources assigned for COM5 and COM6 controllers

	COM5	COM6
Control area	BA+0x00 – BA+ 0x07	BA+0x08 – BA+ 0x0F
ISA bus interrupt line	IRQ7	IRQ9

Mode of each port operation is set by programming the registers of EXAR XR16C2850IM controller.

The maximum baud rate for COM5 and COM6 ports is 3.6 Mbaud. The ports are fully software compatible with the model UART 16550.
The transmitters are controlled in RS-422/485 mode by hardware.
The maximum number of modules that can be connected to the RS-485 network together with the module CPC307, is 128, provided that the input impedance of the RS-485 drivers is minimum 96 kΩ.
For arranging an RS-485 interface, the TX+ and RX+ lines and the TX- and RX- lines on the XP17 connector must be combined.

In module versions older than 4.x a jumper must be installed to pins 3-4 of the XP15 connector for COM5 port and/or to pins 3-4 of the XP20 connector for COM6 port to connect the RX-/RX+ line terminating resistor Rtr.
To connect the Rtt terminating resistor to the TX-/TX+ line a jumper must be installed to pins 1-2 of the XP15 connector for the COM5 port and/or to pins 1-2 of the XP20 connector for the COM6 port (see paragraph 4.3.20 Configuration jumpers).

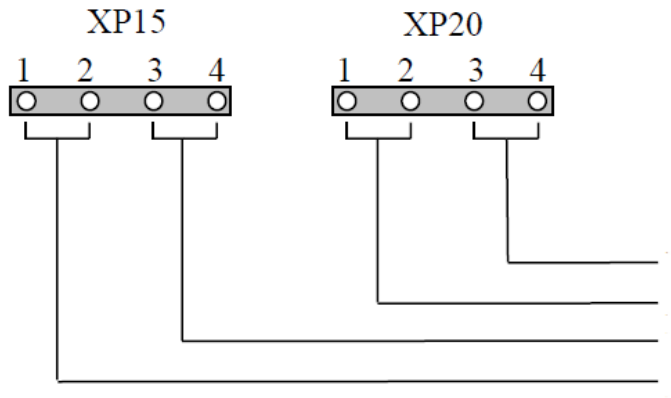


Figure 4.22. a) Pin assignment of the XP15 and XP20 connectors (for module versions older than 4.x)

In module versions 4.x to connect the Rtr terminating resistor to the RX-/RX+ line, a jumper should be installed to pins 5-6 of the XP15 connector for the COM5 port and/or to pins 5-6 of the XP20 connector for the COM6 port.

It is also possible to connect 680 ohm bias resistors.

To connect a 680 ohm VCC bias resistor to the TX-TX+ line a jumper must be installed to pins 1-2 of the XP15 connector for the COM5 port and/or to pins 1-2 of the XP20 connector for the COM6 port.

To connect a 680 ohm GND bias resistor to the TX-/TX+ line a jumper should be installed to pins 3-4 of the XP15 connector for the COM5 port and/or to pins 3-4 of the XP20 connector for the COM6 port.

To connect the Rtt terminating resistor to the TX-/TX+ line it is necessary to simultaneously install 2 x jumpers to pins 1-2 and 3-4 of the XP15 connector for the COM5 port and/or to pins 1-2 and 3-4 of the XP20 connector for the COM6 port.

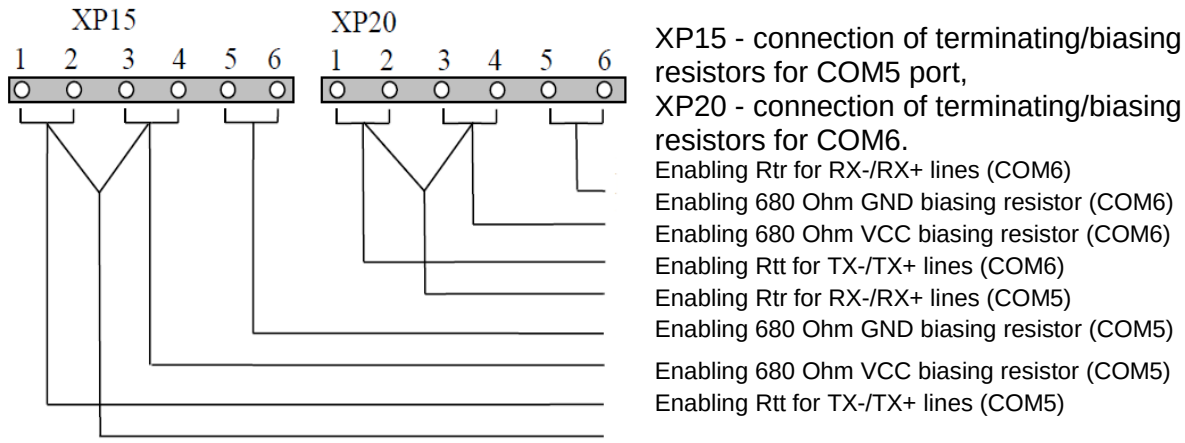


Figure 4.22. b) Pin assignment of the XP15 and XP20 connectors (for module version 4.x)

When the RS-485 network state is inactive, all the drivers are set to the third state, therefore all the nodes are in the receiving mode. Thus, the network state is not defined. If the potential difference at the receiver inputs RX+ and RX- is less than the threshold value of ±200 mV, then the logic level at the receiver output (RX) will be the value of the last received data bit. Safety bias resistors are used to ensure proper voltage levels in the inactive state of the network. A 2.2 kΩ protective bias

resistor (Rcm+) is installed to set the initial high level on the TX+ line. A 2.2 kOhm (Rcm-) protective bias resistor is installed on the TX- line to set the initial low level (Figure 4.23 a) (for module versions older than 4.x)).

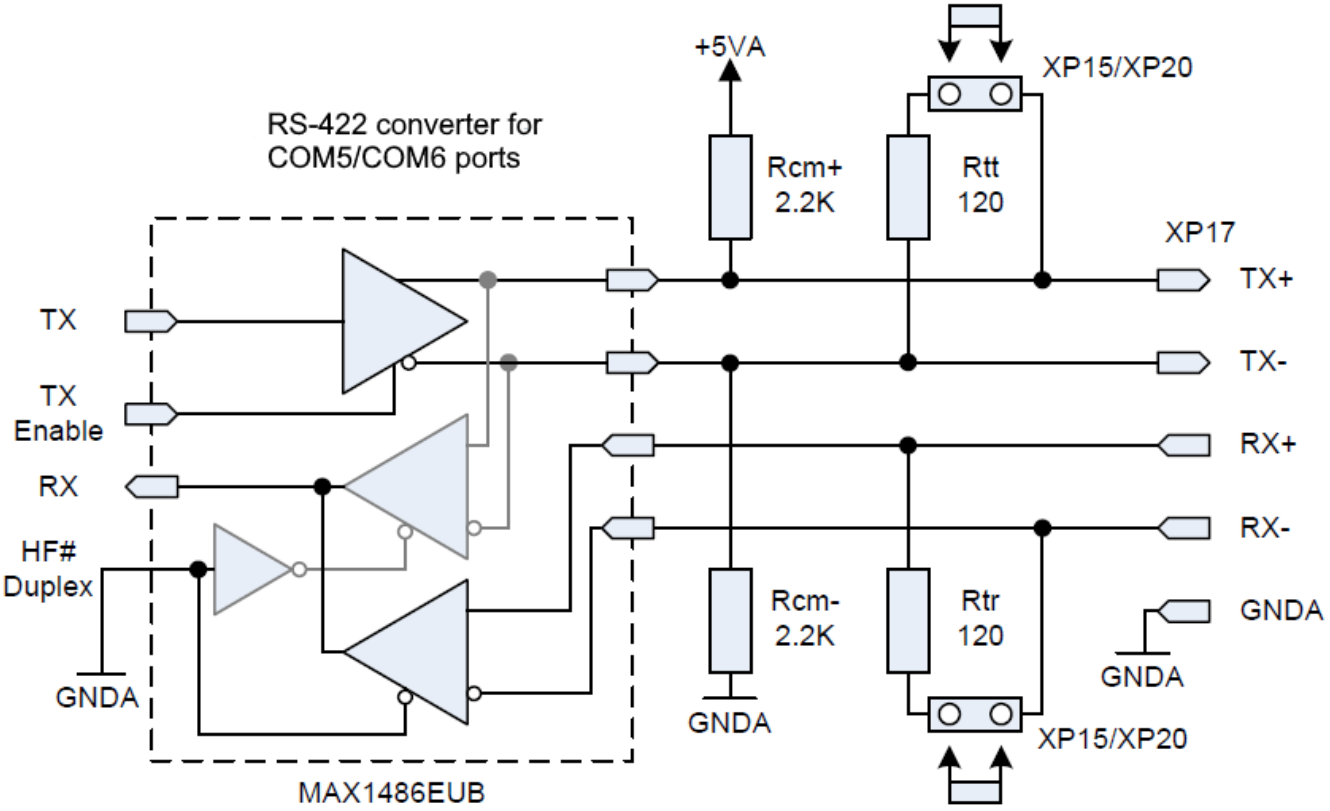


Figure 4.23. a) Transmitter with protective bias elements and terminating resistors (for module versions older than 4.x)

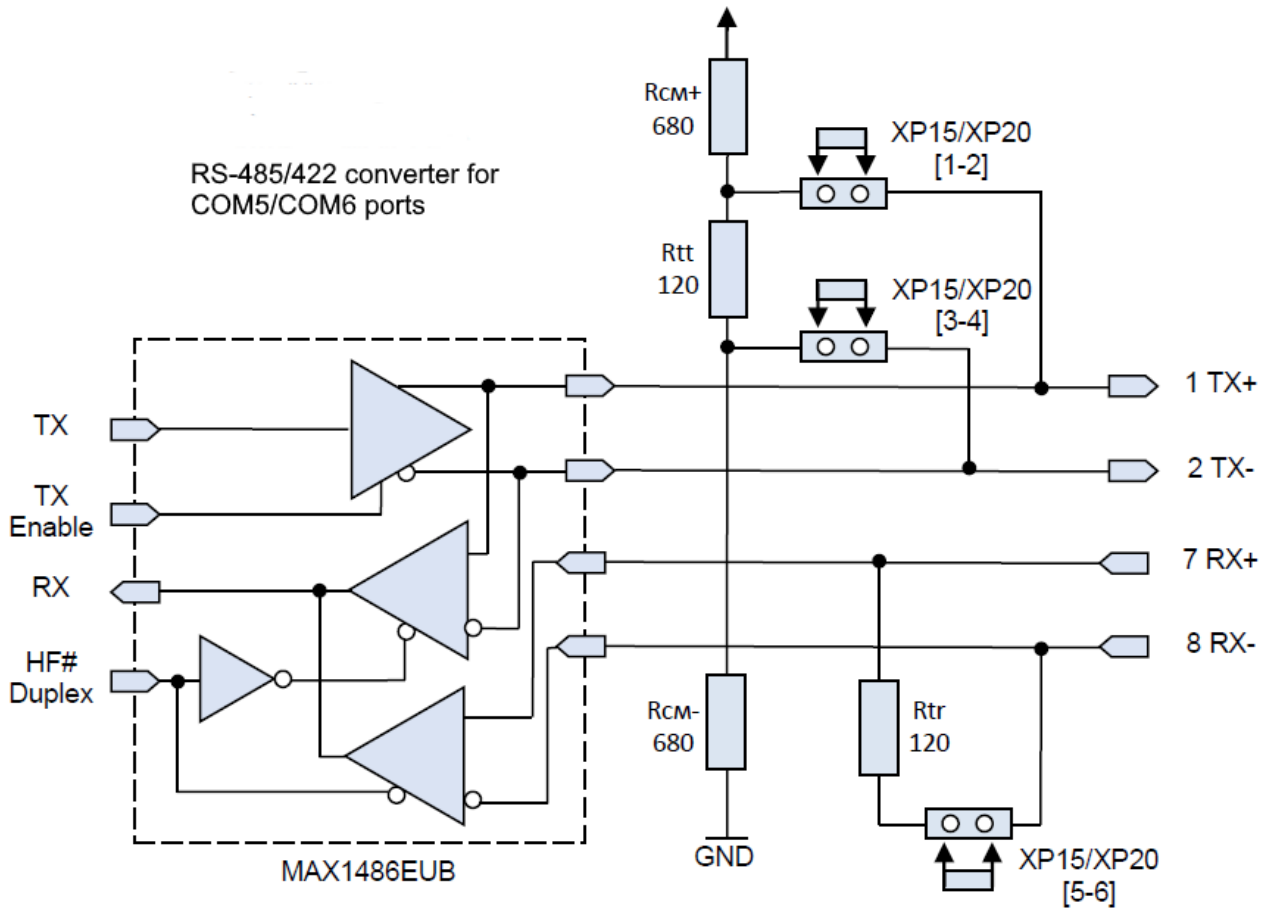


Figure 4.23. b) Transmitter with protective bias elements and terminating resistors (for module version 4.x)

The interfaces are routed to the XP17 connector (IDC2-10, 2-row male connector with a pitch of 2 mm).
Pin assignment of the XP17 connector pin is shown in Table 4.20.
The module has a Leotronics 2073-3102 connector.
The recommended mating part is Leotronics 2039-3101 (ribbon cable press-on socket) or Leotronics 2022-2102 (socket) and 2023-2000 set of contacts.
The maximum number of CPC307 modules combined into a single RS-485 network is 16.

Table 4.20. Pin assignment of the XP17 connector for COM5 and COM6 ports

Pin	Signal	Pin	Signal
1	TX+ (COM5)	2	TX- (COM5)
3	RX+ (COM5)	4	RX- (COM5)
5	GND (COM5)	6	TX+ (COM6)
7	TX- (COM6)	8	RX+ (COM6)
9	RX- (COM6)	10	GND (COM6)

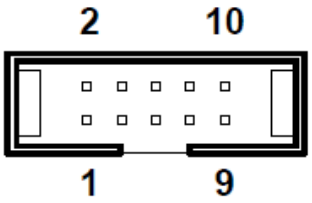


Figure 4.24. Numbering pins of the XP17 connector

4.3.11 Printer Parallel Port (LPT)

The LPT1 parallel port operates in SPP, EPP, ECP mode and has the standard PC/AT standard PC/AT base addresses. Base address and interrupt line selection for the LPT1 port is carried out in the BIOS Setup.

The interface is routed to the part of the XP12 connector (IDC2-20, 2-row male connector with a pitch of 2 mm).

Pin assignment of the XP12 connector related to the LPT interface is shown in Table 4.21.

The module has a Leotronics 2073-3442 connector.

The recommended mating part is Leotronics 2040-3442 (ribbon cable press-on socket) or Leotronics 2022-2442 (socket) and 2023-2000 set of contacts.

Attention!

The +5 V power supply circuit combines homonymous contacts of the XS1 (PCI-104), XS2 (PC-104), and XP22 (additional power connector) connectors and is designed for module's power supply. The +5 V power supply outputs are protected by a 0.5 A fuse. For connected external modules, the recommended current consumption value is not more than 0.4 A. It is not recommended to connect power from interface connectors to more than one external module in order not to overload the power supply circuits of the CPU module.

Table 4.21. Pin assignment of the XP12 for connection of the LPT1 port

Pin	Signal	Pin	Signal
1	STB#	2	AFD#
3	PD0	4	ERR#
5	PD1	6	INIT#
7	PD2	8	SLIN#
9	PD3	10	GND
11	PD4	12	GND
13	PD5	14	GND
15	PD6	16	GND
17	PD7	18	GND
19	ACK#	20	GND

21	BUSY	22	GND
23	PE	24	GND
25	SLCT	26	+5 B

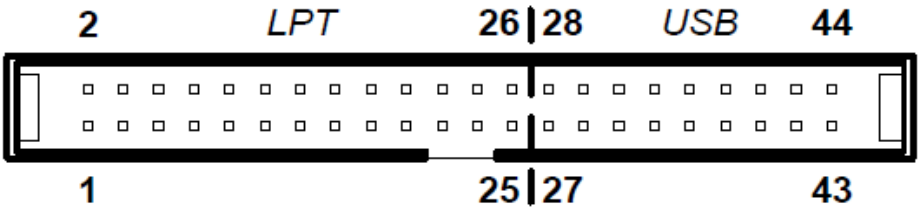


Figure 4.25. Numbering pins of the XP12 connector

4.3.12 PC/104-*plus* connector

4 x expansion cards with the PC/104-plus interface (PCI bus, 32 bits, 33 MHz, +3.3 V) can be connected to the module. Up to 3 x PCI-master devices are supported on the PC/104-plus bus.
The interface is routed to the XS1 connector (PCI-104 connector, 120 pins, 2mm pitch).
The XS1 connector pin assignment and the load-carrying capacity of the PCI bus circuits are given in Table 4.22.
AMP 1375799-1 connector and AMP 1375801-1 organizer are installed on the module.

Table 4.22. Pin assignment of the XS1 connector

Pin	Signal	State	Load-carrying capacity, mA	Pin	Signal	State	Load-carrying capacity, mA
A1	GND	Power supply	–	B1	–	–	–
A2	VI/O	+3,3 V (output)	–	B2	AD2	Input / Output	12
A3	AD5	Input / Output	12	B3	GND	Power supply	–
A4	C/BE0#	Input / Output	12	B4	AD7	Input / Output	12
A5	GND	Power supply	–	B5	AD9	Input / Output	12
A6	AD11	Input / Output	12	B6	VI/O	+3,3 V (output)	–
A7	AD14	Input / Output	12	B7	AD13	Input / Output	12
A8	–	–	–	B8	C/BE1#	Input / Output	12
A9	SERR#	PU (10K)	–	B9	GND	Power supply	–
A10	GND	Power supply	–	B10	PERR#	PU (10K)	–
A11	STOP#	Input / Output	12	B11	–	–	–

A12	–	–	–	B12	TRDY#	Input / Output	12
A13	FRAME#	Input / Output	12	B13	GND	–	–
A14	GND	Power supply	–	B14	AD16	Input / Output	12
A15	AD18	Input / Output	12	B15	–	–	–
A16	AD21	Input / Output	12	B16	AD20	Input / Output	12
A17	–	–	–	B17	AD23	Input / Output	12
A18	IDSEL0	AD12	–	B18	GND	Power supply	–
A19	AD24	Input / Output	12	B19	C/BE3#	Input / Output	
A20	GND	Power supply	–	B20	AD26	Input / Output	12
A21	AD29	Input / Output	12	B21	+5 V	Power supply	–
A22	+5 V	Power supply	–	B22	AD30	Input / Output	12
A23	REQ0#	Input	–	B23	GND	Power supply	–
A24	GND	Power supply	–	B24	REQ2#	Input	–
A25	GNT1#	Output	12	B25	VI/O	+3,3 V (output)	–
A26	+5 V	Power supply	–	B26	CLK0	Output	12
A27	CLK2	Output	6	B27	+5 V	Input	–
A28	GND	Power supply	–	B28	INTD#	Input	–
A29	+12 V	–	–	B29	INTA#	Input	–
A30	-12 V	–	–	B30	–	–	–
Pin	**Signal**	**State**	**Load-carrying capacity, mA**	**Pin**	**Signal**	**State**	**Load-carrying capacity, mA**
C1	+5 V	Power supply	–	D1	AD0	Input / Output	12
C2	AD1	Input / Output	12	D2	+5 V	Power supply	–
C3	AD4	Input / Output	12	D3	AD3	Input / Output	12
C4	GND	Power supply	–	D4	AD6	Input / Output	12
C5	AD8	Input / Output	12	D5	GND	Power supply	–
C6	AD10	Input / Output	12	D6	M66EN (GND)	–	–
C7	GND	Power supply	–	D7	AD12	Input / Output	12

C8	AD15	Input / Output	12	D8	–	–	–
C9	–	–	–	D9	PAR	Input / Output	12
C10	–	–	–	D10	–	–	–
C11	LOCK#	PU (10K)	–	D11	GND	Power supply	–
C12	GND	Power supply	–	D12	DEVSEL#	Input / Output	12
C13	IRDY#	Input / Output	12	D13	–	–	–
C14	–	–	–	D14	C/BE2#	Input / Output	12
C15	AD17	Input / Output	12	D15	GND	Power supply	–
C16	GND	Power supply	–	D16	AD19	Input / Output	12
C17	AD22	Input / Output	12	D17	–	–	–
C18	IDSEL1	AD13	–	D18	IDSEL2	AD14	–
C19	VI/O	+3,3 V (output)	–	D19	IDSEL3	AD15	–
C20	AD25	Input / Output	12	D20	GND	Power supply	–
C21	AD28	Input / Output	12	D21	AD27	Input / Output	12
C22	GND	Power supply	–	D22	AD31	Input / Output	12
C23	REQ1#	Input	–	D23	VI/O	+3,3 V (output)	–
C24	+5 V	Power supply	–	D24	GNT0#	Output	12
C25	GNT2#	Output	12	D25	GND	Power supply	–
C26	GND	Power supply	–	D26	CLK1	Output	12
C27	CLK3	Output	6	D27	GND	Power supply	–
C28	+5 V	Power supply	–	D28	RST#	Output	12
C29	INTB#	Input	–	D29	INTC#	Input	–
C30	GNT3#	PU (10K)	–	D30	GND	Power supply	–

The “State” column indicates the direction of data transmission for the case when the module is a bus master.

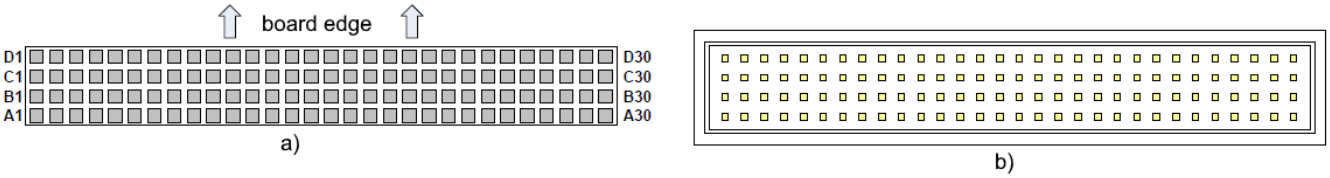


Figure 4.26. PCI-104 XS1 connector: a) module top view; b) module bottom view with organizer mounted on the connector

Restrictions regarding installation of particular PC/104+ expansion boards on the module are described in Section 7.

4.3.13 PC/104 connector

It is possible to connect additional expansion boards with the PC/104 interface (ISA bus, 8/16 bits, 8.3/16.6 MHz, DMA support) to the module. The master mode is not supported for PC/104 bus.
The interface is routed to the XS2 connector (PC-104 connector, 104 pins, 2.54 mm pitch).
The assignment of the XS2 connector pins and the default load-carrying capacity of the ISA bus circuits are given in Table 4.23.
The module has an AMP 1375795-5 connector and an AMP 1445251-1 organizer.

Table 4.23. Pin assignment of the XS2 connector

Pin	Signal	State	Load-carrying capacity, mA	Pin	Signal	State	Load-carrying capacity, mA
A1	IOCHK#	Input	–	B1	GND	Power supply	–
A2	SD7	Input / Output	16	B2	RESET	Output	16
A3	SD6	Input / Output	16	B3	+5 V	Power supply	–
A4	SD5	Input / Output	16	B4	IRQ9	Input	–
A5	SD4	Input / Output	16	B5	–	–	–
A6	SD3	Input / Output	16	B6	DRQ2	Input	–
A7	SD2	Input / Output	16	B7	-12 V	–	–
A8	SD1	Input / Output	16	B8	0WS#	Input	–
A9	SD0	Input / Output	16	B9	+12 V	–	–
A10	IOCHRDY	Input	16	B10	GND	Power supply	–
A11	AEN	Output	16	B11	SMEMW#	Output	16
A12	SA19	Output	16	B12	SMEMR#	Output	16
A13	SA18	Output	16	B13	IOW#	Output	16
A14	SA17	Output	16	B14	IOR#	Output	16
A15	SA16	Output	16	B15	DACK3#	Output	8

A16	SA15	Output	16	B16	DRQ3	Input	–
A17	SA14	Output	16	B17	DACK1#	Output	8
A18	SA13	Output	16	B18	DRQ1	Input	–
A19	SA12	Output	16	B19	REFRESH#	Output	8
A20	SA11	Output	16	B20	CLK	Output	8
A21	SA10	Output	16	B21	IRQ7	Input	–
A22	SA9	Output	16	B22	IRQ6	Input	–
A23	SA8	Output	16	B23	IRQ5	Input	–
A24	SA7	Output	16	B24	IRQ4	Input	–
A25	SA6	Output	16	B25	IRQ3	Input	–
A26	SA5	Output	16	B26	DACK2#	Output	8
A27	SA4	Output	16	B27	TC	Output	8
A28	SA3	Output	16	B28	BALE	Output	16
A29	SA2	Output	16	B29	+5 V	Power supply	–
A30	SA1	Output	16	B30	OSC	Output	16
A31	SA0	Output	16	B31	GND	Power supply	–
A32	GND	Power supply	–	B32	GND	Power supply	–
Pin	**Signal**	**State**	**Load-carrying capacity, mA**	**Pin**	**Signal**	**State**	**Load-carrying capacity, mA**
C0	GND	Power supply	–	D0	GND	Power supply	–
C1	SBHE#	Output	8	D1	MEMCS16#	Input	8
C2	LA23	Output	8	D2	IOCS16#	Input	8
C3	LA22	Output	8	D3	IRQ10	Input	–
C4	LA21	Output	8	D4	IRQ11	Input	–
C5	LA20	Output	8	D5	IRQ12	Input	–
C6	LA19	Output	8	D6	IRQ15	Input	–
C7	LA18	Output	8	D7	IRQ14	Input	–
C8	LA17	Output	8	D8	DACK0#	Output	8
C9	MEMR#	Output	16	D9	DRQ0	Input	–
C10	MEMW#	Output	16	D10	DACK5#	Output	8
C11	SD8	Input / Output	16	D11	DRQ5	Input	–
C12	SD9	Input / Output	16	D12	DACK6#	Output	8
C13	SD10	Input / Output	16	D13	DRQ6	Input	–

C14	SD11	Input / Output	16	D14	DACK7#	Output	8
C15	SD12	Input / Output	16	D15	DRQ7	Input	–
C16	SD13	Input / Output	16	D16	+5 V	Power supply	–
C17	SD14	Input / Output	16	D17	MASTER#	–	–
C18	SD15	Input / Output	16	D18	GND	Power supply	–
C19	KEY	–	–	D19	GND	Power supply	–

The “State” column indicates the direction of data transmission for the case when the module is a bus master.

Figure 4. 27. Numbering of the XS2 connector pins: a) top view of the module; b) bottom view of the module with the organizer mounted on the connector

Restrictions regarding installation of particular PC/104 expansion boards on the module are described in Section 7.

4.3.14 CAN-interfaces

The CPC307 module is equipped with two SJA1000T controller chips, compatible with the CAN 2.0b interface specification, and supports two independent CAN interface ports. There is a possibility of a software reset of the CAN controllers of each interface. The base address (BA) for the serial ports is selected by programming the registers of the Vortex86DX SoC. The interrupt lines are set by the hardware.
The maximum baud rate for the CAN1 and CAN2 ports is 1 Mb/s.
For more details see paragraph **4.2 Address space allocation**.
Table 4.24 shows the assigned resources of each CAN controller.

Table 4.24. Assigned resources of the CAN1 and CAN2 controllers

	CAN1	**CAN2**
Control area	BA+0x000 – BA+ 0x0FF	BA+0x200 – BA+ 0x2FF
Reset area (when these addresses are accessed, the corresponding CAN controller is reset)	BA+0x100 – BA+ 0x1FF	BA+0x300 – BA+ 0x3FF
ISA bus interrupt line	IRQ10	IRQ11

The ports provide the ability to connect devices with an isolated CAN interface.
The module provides isolation of interfaces up to 500 V.
To connect the Rt terminating resistor to the CANL/CANH line, you must set a jumper to pins 3-4 (3-4 and 5-6 for 4.x module versions) of the XP4 connector for the CAN1 port.
To enable the high-speed mode of the line driver, it is required to set a jumper to pins 1-2 of the XP4 connector for the CAN1 port.

To connect the Rt terminating resistor to the CANL/CANH line, you must set a jumper to pins 3-4 (3-4 and 5-6 for 4.x module versions) of the XP8 connector for the CAN2 port.
To enable the high-speed mode of the line driver, it is required to set a jumper to pins 1-2 of the XP8 connector for the CAN2 port.

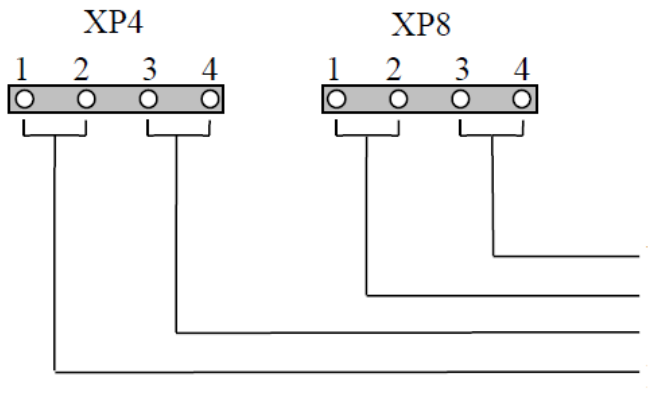


Figure 4.28. a) Pin assignment of the XP4 and XP8 connector (for module versions lower than 4.x)

The interfaces are routed to the XP5 connector (IDC2-10, 2-row male connector with a pitch of 2 mm).
Pin assignment of the XP5 connector is shown in Table 4.25.
The module has a Leotronics 2073-3102 connector.
The recommended mating part is Leotronics 2039-3101 (ribbon cable press-on socket) or Leotronics 2022-2102 (socket) and 2023-2000 set of contacts.

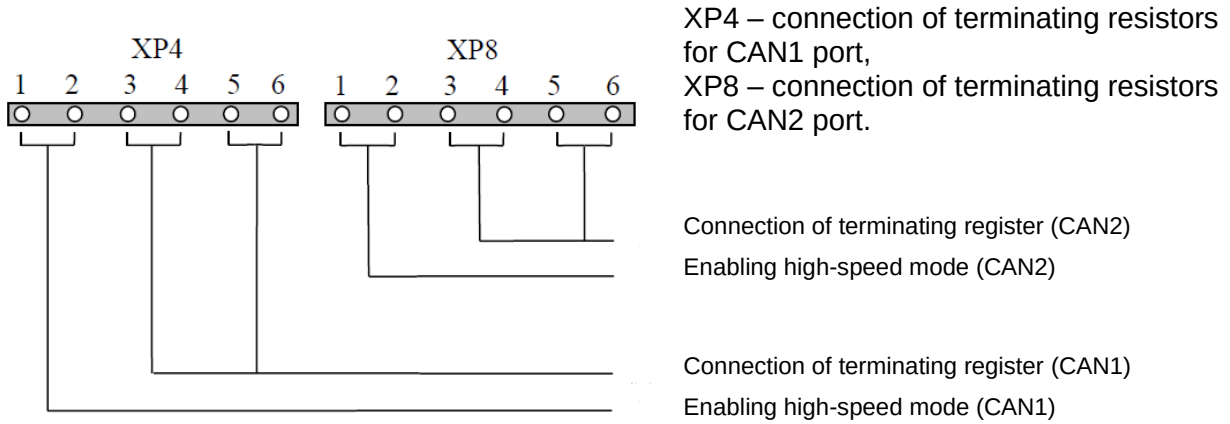


Figure 4.28.b) Pin assignment of the XP4 and XP8 connectors for module versions 4.x

Table 4.25. Pin assignment of the XP5 connector for CAN1 and CAN2 ports

Pin	Signal	Pin	Signal
1	CANH (CAN1)	2	CANL (CAN1)
3	GND_CAN1	4	–
5	–	6	–
7	–	8	CANH (CAN2)

9	CANL (CAN2)	10	GND_CAN2

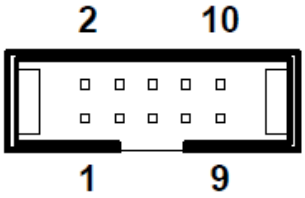


Figure 4.29. Numbering pins of the XP5 connector

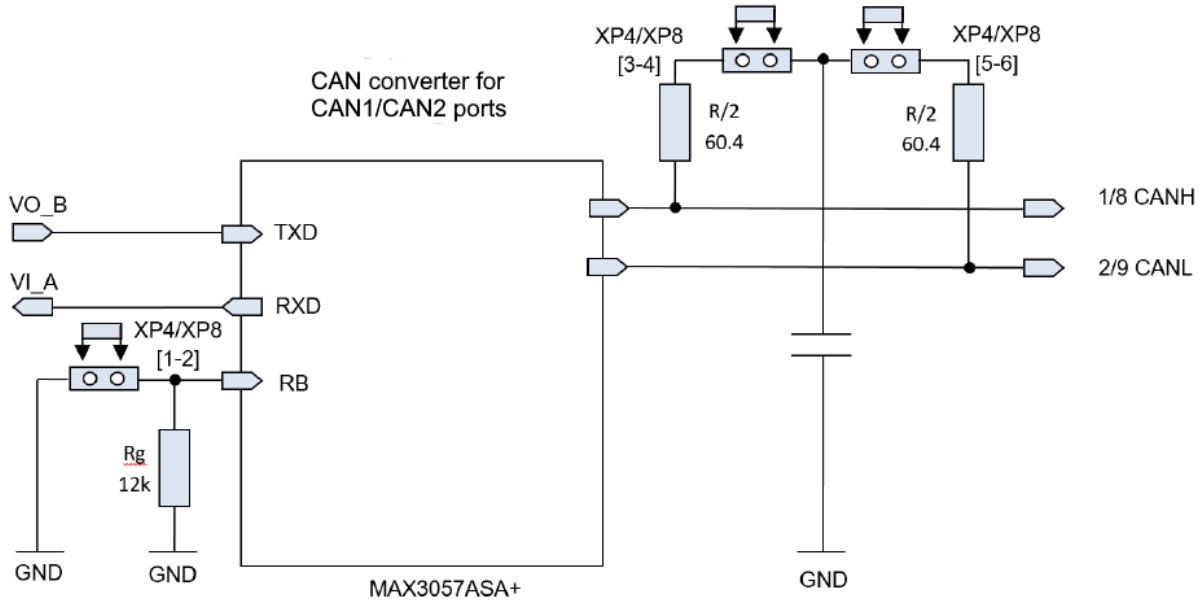


Figure 4.30. Connection of the fail-safe biasing on CAN line

4.3.15 WDT watchdog timers

The module uses 3 x WDT (Watchdog Timer) timers.
The first two timers with programmable 30.5µs to 512s interval (WDT0, WDT1) are integrated into the Vortex86DX SoC. The timers are controlled through the internal registers of the processor (paragraph **4.3.15.1 WDT0, WDT1 watchdog timers**).
A third timer with a fixed interval of 1.6 seconds (WDT2) is integrated into the ADM706T power supply supervisor chip. The WDT2 response times are fixed by a trigger, the state of which can be seen after resetting the module, and this will also be signaled by a green LED HL2. The timer is controlled via lines 1-3 of the GPIO1 port of the Vortex86DX chip (paragraph **4.3.15.2 WDT2 watchdog**).

4.3.15.1 WDT0, WDT1 watchdog timers

The Vortex86DX SoC contains 2 x configurable watchdog timers.
The WDT0 timer registers are accessed through port 65h, port 22h (Address Register) and port 23h (Data Register). To access the registers, the address of the port must be written to port 22h, read and / or write of registers values is done through port 23h.

Table 4.26 provides a detailed description of the WDT0 watchdog timer control registers.
The registers of the timer WDT1 are accessed through the ports 67h - 6Dh.
Table 4.27 provides a detailed description of the WDT1 watchdog timer control registers.

Table 4.26. Description of the WDT0 watchdog timer control registers

Port address	Bit	Access type	Description
WDT0 Restart Register			
65h	7:0	W	Writing to this port will restart the WDT0 timer. Reading is not possible.
WDT0 Control Register (value after 40h reset)			
Address register (22h) = 37h	7	RO	Reserved
	6	R/W	WDT0 timer is enabled 0 – disabled 1 – enabled
	5:0	RO	Reserved
WDT0 event selection register (value after D0h reset)			
Address register (22h) = 38h	7:4	RW	Event selection at the end of WDT0 timer count Bits [7:4] – signal: 0000 – reserved 0001 – IRQ[3] 0010 – IRQ[4] 0011 – IRQ[5] 0100 – IRQ[6] 0101 – IRQ[7] 0110 – IRQ[9] 0111 – IRQ[10] 1000 – IRQ[11] 1001 – IRQ[12] 1010 – IRQ[14] 1011 – IRQ[15] 1100 – NMI 1101 – system reset 1110 – reserved 1111 – reserved
	3:0	RO	Reserved
Register 0 of WDT0 timer (value after 00h reset)			
Address register (22h) = 39h	7:0	R/W	Bits [7:0] of WDT0 timer, resolution – 30.5 µs
Register 1 of WDT0 timer (value after 00h reset)			
Address register (22h) = 3Ah	7:0	R/W	Bits [15:8] of WDT0 timer, resolution – 30.5 µs
Register 2 of WDT0 timer (value after 20h reset)			
Address register (22h) = 3Bh	7:0	R/W	Bits [23:16] of WDT0 timer, resolution – 30.5 µs
WDT0 state register (value after 00h reset)			

Address register (22h) = 3Ch	7	R/WC	WDT0 timer status flag 0 – timer was not triggered 1 – timer was triggered (writing “1” to this bit resets the flag)
	6	W	Writing “1” will make the WDT0 timer to restart. Writing “0” to this bit or reading is not allowed
	5:0	RO	Reserved

Table 4.27. Description of the WDT1 watchdog timer control registers

Port address	Bit	Access type	Description
WDT1 restart register			
67h	7:0	W	Writing to this port will restart the WDT1 timer. Reading is not possible.
WDT1 control register (value after 00h reset)			
68h	7	RO	Reserved
	6	R/W	Enabling WDT1 timer operation 0 – disabled 1 – enabled
	5:0	RO	Reserved
WDT1 event selection register (value after 00h reset)			
69h	7:4	RW	Event selection at the end of WDT1 timer count Bits [7:4] – signal: 0000 – reserved 0001 – IRQ[3] 0010 – IRQ[4] 0011 – IRQ[5] 0100 – IRQ[6] 0101 – IRQ[7] 0110 – IRQ[9] 0111 – IRQ[10] 1000 – IRQ[11] 1001 – IRQ[12] 1010 – IRQ[14] 1011 – IRQ[15] 1100 – NMI 1101 – system reset 1110 – reserved 1111 – reserved
	3:0	RO	Reserved
Register 0 of WDT1 timer (value after 00h reset)			
6Ah	7:0	R/W	Bits [7:0] of WDT1 timer, resolution – 30.5 µs
Register 1 of WDT1 timer (value after 00h reset)			
6Bh	7:0	R/W	Bits [15:8] of WDT1 timer, resolution – 30.5 µs
Register 2 of WDT1 timer (value after 00h reset)			

6Ch	7:0	R/W	Bits [23:16] of WDT1 timer, resolution – 30.5 µs
WDT1 state register (value after 00h reset)			
6Dh	7	R/WC	WDT1 timer status flag 0 – timer was not triggered 1 – timer was triggered (writing “1” to this bit resets the flag)
	6:0	RO	Reserved

4.3.15.2 WDT2 watchdog timer

The WDT2 watchdog functions are performed by the ADM706T chip. The timer functions are controlled through GPIO1 lines 1, 2, 3, 4 of the Vortex86DX SoC chip:
GPIO1 line 1 (output) - WDT2 watchdog timer reset;
GPIO1 line 2 (output) – Enabling WDT2 watchdog timer. “1” - enabled, “0” - disabled;
GPIO1 line 3 (output) - In module version 1.0 this pin is not used (Watchdog state trigger resets to “0”);
GPIO1 line 4 (input) - Watchdog state. “1” - was triggered, “0” - was not triggered.
In module versions lower than 4.x, the WDT2 watchdog timer can be hardware disabled by setting a jumper to the XP26 connector. In module versions 4.x, the opposite is true: setting a jumper to the XP26 enables the WDT2 watchdog timer, while removing the jumper disables it.
For a more detailed description of GPIO ports see paragraph **4.3.19 GPIO Ports**.

4.3.16 RTC, CMOS, FRAM, hardware reset and BIOS backup

Standard, IBM PC-compatible real time clock (RTC - Real Time Clock) is used in the module. Clock operation in the off state of the module is provided by a 3V CR2032 (Renata) DC battery, installed in the X1 holder.

Attention!
In order to ensure the accuracy of the real time clock, it is recommended to synchronize it with the accurate readings at least once a day. It is recommended to synchronize the real time clock after transportation and storage.

4.3.16.1 BIOS backup

Two copies of BIOS are stored in the module (for versions lower than 4.x) - the main and backup BIOS. When you turn on the power supply the module always boots from the main BIOS copy. In the event of actuation of the external watchdog in the ADM706T power supply supervisor chip, the module will restart.
If the XP21 jumper is removed, the module is always booted from the main BIOS copy (paragraph **4.3.20 Configuration jumpers**). When the XP21 jumper is installed and the watchdog timer is triggered the module will restart from the BIOS backup copy. Further watchdog triggering will also be done from the backup copy.

When booting from the BIOS backup copy, you can resume booting from the main copy by one of the following ways:

- resetting the module's operation with the SW1 switch (RESET#);

- resetting module operation by external opto-isolated reset with a jumper installed on pins 1-2 of the XP25 connector (paragraph **4.3.7 Opto-isolated reset/interrupt**);

- jumper installed or short-term closure of pins 1-2 of the XP27 connector, followed by restarting the module;

- setting GPIO1 port line 3 to “0” followed by restarting the module (see paragraph **4.3.19 GPIO Ports**);

- de-energizing the module. The module always boots from the main BIOS copy when power is on.

Indication of watchdog timer triggering and indication of booting from the BIOS backup copy are available by pressing the LED on pins 5-6 of the XP3 connector (paragraph **4.3.21 LED indication**).

BIOS settings can be changed only via the BIOS Setup menu.

Note
For module version 4.x there is no BIOS backup.

4.3.16.2 CMOS memory and replaceable CR2032 battery

A replaceable 3 B CR2032 (Renata) power supply battery installed in the X1 holder ensures proper functioning of the real-time clock (RTC) and that the BIOS settings are stored in the CMOS memory when the module is powered off.
BIOS settings are automatically duplicated and stored in FRAM and automatically restored at power-up if data in CMOS memory is damaged. With this feature you can use the module without a CR2032 battery installed on it, but the system time and date are not saved.
The capacity of the replaceable DC battery is 235 mA/h. The battery current consumption when the module is turned off is about 2 μA.
Expected/typical battery life is approximately 10 years at an ambient temperature of 23ºC. However, the battery life is highly dependent on operating temperature.
It is recommended to replace the battery every 5 years of operation/storage of the module without waiting for the battery life to expire.
The proper polarity (“+” at the top) must be observed when replacing the battery. The used battery must be disposed of in accordance with the appropriate regulations.
The CMOS_RST utility can be found on the FTP server at:
ftp://ftp.prosoft.ru/pub/Hardware/Fastwel/CPx/CPC306/Software/Drivers/DOS/UTILS/
If the current CMOS settings do not allow the module to function properly during operation and it is not possible to enter the BIOS SETUP menu to change the settings, you switch the settings to the “default” state. This can be done with this utility by performing the following sequence of actions:
- turn the module off, connect the COM1 port (XP9 connector) of the module to the COM1 port of a personal computer through the “null-modem” cable[1] and ACS00023 cable (FAPI.685611.082) from the module delivery checklist;
- start on the PC (under Windows 2000/XP) the program CMOS_RST.EXE. This program will send a command to the port for setting the BIOS Setup values to the default. Turn the module on.
Remote CMOS Reset for Windows 2000/XP.
Version 1.0 Copyright (C) 2000, 2007 Fastwel Inc.
Sending "reset" sequence through COM1. Press a key to abort

- switch on the module's power.
- enter the module's BIOS SETUP and set the required BIOS settings.

4.3.16.3 Operation with FRAM

Note
The least-significant 1 KB of the FRAM memory is reserved! Writing to this area may cause non-stable operation of the module.

The module has 32 KB of non-volatile FRAM memory. The user has access to the most-significant 31 KB. The memory is accessed through the SPI interface.
The user can address the FRAM memory directly through the registers of the SPI interface. More detailed information can be found in the description on the Vortex86DX SoC (A9121) and FRAM memory, which can be found in the relevant folder on the FTP server.
Working with the memory FRAM by BIOS is carried out through the function INT 17h (service interrupt FRAM is combined with the interrupt printer service).
To call the FRAM service, an interrupt INT 17h with a parameter in the register AH = 0ADh is used. The values of other parameters passed in the processor registers are given below.
Where the function number (AL) is specified incorrectly, this will make to return AX = -1 (0FFFFh).
FRAM memory structure:

```
_FRAM     STRUCT
          db   256 dup (0)   ; Reserve for storing CMOS copy
dADCVS  dd  4*8*2 dup (0) ; Reserved for CPC306
dADCCS  dd  2*8*2 dup (0) ; Reserved for CPC306
dDACVS  dd  3*2*2 dup (0) ; Reserved for CPC306
dSerNum  dd  0                ; Serial number of the module
```

---

1) The standard cable is not included in the delivery checklist and optional accessories of the module, to be purchased as an option.

```
wMac       dw     -1,-1,-1     ; MAC address of the embedded Ethernet controller
wCheck     dw      0           ; Array checksum
bUser db    ?                  ; Start of the user area

_FRAM      ENDS
-------------------------------------------------------
Obtaining serial number of the module.
Input:    AL = 6
Output: AX = result code (0 - no error)
   CX:DX = serial number.

-------------------------------------------------------
-------------------------------------------------------
Reading MAC address of embedded Ethernet from FRAM field.
Input:    AL = 8
Output: AX = result code (0 - no error)
```

SI:CX:DX = MAC-address.

The function returns the value stored in the FRAM MAC address field. The actual value, used by the controller may be different if it has been overwritten directly into the registers of the controller by the application software.

Verification of the checksum of the parameter array in FRAM.
Input: AL = 0Ah
Output: AX = checksum (0 - no error)
The function returns the value of the checksum of the parameters array in the FRAM.

Updating the checksum of the parameters array in FRAM.
Input: AL = 0Bh
Output: AX = result code (0 – no error)
The function recalculates and updates the checksum of all bytes of the parameter array in FRAM. The function must be called after changing the parameters.

Reading user data from FRAM.
Input: AL = 0Ch
BX = Address of data beginning in the FRAM user area
CX = number of bytes to be read
DS:DX = indicator to read buffer
Output: AX = result code (0 – no error, -2 (0FFFEh) - parameter error, wrong address)
BX = Maximum address allowed (user area size-1)
CX = Number of actually read bytes
The function reads the specified bytes of the user FRAM area into the buffer of the calling program.

Writing user data to FRAM.
Input: AL = 0Dh
BX = Address of data beginning in the FRAM user area
CX = number of the bytes written
DS:DX = indicator to the data to be written
Output: AX = result code (0 – no error, -2 (0FFFEh) - parameter error, wrong address)
BX = Maximum address allowed (user area size-1)
CX = Number of bytes actually written
The function writes data to the user FRAM area

Reading flags of the test mode.
Input: AL = 0Eh
BX = 0ABCDh (key)
Output: AX = test mode flags
The function returns the value of the test mode flags:
bit 7: 0 = normal mode (bit values 0 -1 have no effect), 1 = test mode

bits 6-2:reserve
bit 1: 0 = set IDE controller mode according to Setup settings,
1 = set SD Card mode regardless of Setup settings
bit 0: 0 = use the current Setup parameters during booting,
1 = set the default Setup parameters at booting.

Writing test flags.

Input: AL = 0Fh
BX = 0ABCDh (key)
DX = new value of test mode flags

Output: AX = result code (0 – no error)

The function changes the value of the test flags:

bit 7: 0 = normal mode (bit values 0 -1 have no effect), 1 = test mode
bits 6-2: reserve
bit 1: 0 = set the IDE controller mode according to the Setup settings,
1 = set SD Card mode regardless of Setup settings
bit 0: 0 = use the current Setup parameters during booting,
1 = set the default Setup parameters at booting.

4.3.16.4 BIOS update

4.3.16.4.1 BIOS update for module versions lower than 4.x

The BIOS backup mechanism for module versions lower than 4.x allows you to remotely update the main BIOS copy without the risk of the module malfunctioning if the update fails (in case of a power failure, invalid BIOS image file loaded, etc.).
The current versions of the BIOS image files for the CPC307 module are available on the network file servers of the manufacturer and the official distributor, and are also provided upon the relevant request to the manufacturer's technical support service.
The main BIOS copy is stored in the parallel FLASH chip connected to the ISA bus - the AM29F040B-55EF, 4MB Flash Memory chip.
The backup copy is stored in the FLASH memory integrated into the Vortex86DX SoC and connected to the SPI interface. The backup copy is designed to restore a damaged main BIOS copy (e.g., if a BIOS update attempt fails).

When updating BIOS with the use of the integrated console I/O (paragraph **5.2.3 Remote Access Configuration** (Configuration of Console I/O settings), please note that after image update and reboot, optimal (factory default) BIOS Setup settings will be loaded. If the module is rebooted from the upgraded to the previous BIOS version, the optimal (factory) BIOS Setup settings will also be loaded. In both cases, the console I/O settings will be changed to the factory settings (mode Redirection After BIOS POST = "Boot Loader"). Therefore, if you want to use the integrated BIOS, you must enter BIOS Setup each time you boot up the module during the BIOS update procedure and set the required settings for the console I/O and BIOS as a whole. It is allowed to use the console I/O by means of the OS so that you don't have to change the BIOS Setup settings every time, which will simplify the procedure of updating the both BIOS copies.
To update the main and then the backup BIOS copy it's necessary to install the jumper XP21 and not to install jumper XP26 (see paragraph **4.3.20 Configuration jumpers**).

To update the main BIOS copy you need to perform the following actions:

1. Turn on the CPC307 module and boot in the standard mode using the main BIOS copy.
2. Copy the VXDXBIOS folder from the relevant section of the FTP server (ftp://ftp.prosoft.ru/pub/Hardware/Fastwel/CPx/CPC307/Software/).
Place the updated BIOS image (e.g. c307v310.bin) in the copied folder.
3. Run the BIOS main copy updater from the VXDXBIOS folder. You must specify the BIOS image file name for the update as the parameter:
C:\VXDXBIOS\vxdxbios.exe c307v311.bin
If the update is successful the program will show the following messages:

```
Load file C:\VXDXBIOS\c307v311.bin...
START FLASH ERASE
FLASH ERASE OK. ERASE TIME 4.62 S
FLASH WRITE OK
FLASH VERIFY OK
AM29F040B loaded successfully
```

4. After updating the main BIOS copy you must restart the module. To do this, just power off and then power on the module, or press the SW1 reset key, or reset the module via the opto-isolated reset signal.
After resetting the module, the optimal (factory) BIOS Setup settings can be loaded. If necessary, enter the BIOS Setup, change the required parameters, save and exit (paragraph 5.7 Exit).

5. Make sure that the module is booted from the main BIOS copy:

a. jumper XP21 is installed and jumper XP26 is removed. The WDT2 watchdog timer must not be triggered during booting (paragraph **4.3.15.2 WDT2 watchdog timer**). Make sure that WDT2 has not been triggered, which can be verified by the LED connected to the XP3 connector (paragraph **4.3.21 LED indication**). You can also check the date and version of the BIOS when going through the POST procedure and in the BIOS Setup menu (**Section 5 Basic Input/Output System (BIOS)**).

b. XP21 jumper is removed or both XP21 and XP26 jumpers are installed at the same time. The module always boots from the master copy only. If the module boots, the upgrade is successful.

If the module boots from the main BIOS copy, then the upgrade was successful.

To update the BIOS backup copy you must perform the following steps:

1. Install the jumper XP21, and do not install jumper XP26. Otherwise the backup copy cannot be updated.

2. Turn on the CPC307 module and boot up in a routing mode from the main BIOS copy. The WDT2 watchdog timer must not be triggered during the boot (par. **4.3.15.2 WDT2 watchdog timer**). You can verify that WDT2 has not been triggered by the LED indication connected to the XP3 connector (paragraph **4.3.21 LED indication**). You can also check the date and version of the BIOS when going through the POST procedure and in the BIOS Setup menu (Section **5 Basic Input/Output System (BIOS)**).

Updating the BIOS backup copy is prohibited if the module doesn't boot from the main BIOS copy.

3. Copy the SPIFLASH folder from the FTP server to the module's boot disk. Place the updated BIOS image (e.g. c307v310.bin) into the copied folder.

4. Make sure the XP21 jumper is installed. The XP26 jumper must be removed.

5. Run the WDTRST.EXE program to activate the WDT2 timer and reboot to the BIOS backup (located in the SPIFLASH folder).

C:\SPIFLASH\wdtrst.exe

After the module reboot, the optimal (factory default) BIOS Setup settings can be loaded. If necessary, enter the BIOS Setup, change the necessary parameters, save and exit (paragraph 5.7 Exit).

6. Start BIOS update program from the SPIFLASH folder with the “u” key and specify the updated BIOS image:
C:\SPIFLASH\spiflash.exe u c307v311.bin
If the update is successful, the program will display the following messages:
SPIFLASH 1.11 (May 21, 2008)
(C) Copyright 2007 DMP Electronics Inc.
CPU name = Vortex86DX
SPI base address = fc00
send RDID cmd
Device ID=c2 20 15
Flash type = MX25L1605, ok
Update flash rom data from c307v311.bin:
ADDR : 40000/40000
189 blank data block(s) skipped
Ok

7. After update of the BIOS backup copy you need to run the WDTRST.EXE program in order to restart the module from the BIOS backup copy and verify the correctness of the update!

After the module reboot, the optimal (factory default) BIOS Setup settings can be loaded. If necessary, enter the BIOS Setup, change the necessary parameters, save and exit (paragraph 5.7 Exit).

If the module boots, the BIOS backup copy is updated successfully.

If updating the main BIOS copy led to an error and the module fails to boot (no information about the POST procedure being passed, and the console output was enabled), or the WDT2 watchdog timer goes off (jumper XP26 is removed, the module is periodically reset), in this case you must:
1. Set the XP21 jumper and remove the XP26 jumper.

2. Power on the CPC307 module and boot from the BIOS backup copy (WDT2 watchdog will be triggered if the main BIOS copy is damaged).

After the module reboot, the optimal (factory default) BIOS Setup settings can be loaded. If necessary, enter the BIOS Setup, change the necessary parameters, save and exit (paragraph 5.7 Exit).

3. Run the main BIOS update program from the VXDXBIOS folder. You will need to specify the file name of the BIOS image for updating as the parameter:

C:\VXDXBIOS\vxdxbios.exe c307v311.bin
If the update is successful the program will show the following messages:
Load file C:\VXDXBIOS\c307v311.bin...
START FLASH ERASE
FLASH ERASE OK. ERASE TIME 4.62 S
FLASH WRITE OK
FLASH VERIFY OK
AM29F040B loaded successfully.

6. After updating the main BIOS copy you need to restart the module. To do so, just power off and then power on the module, or press the SW1 reset key, or reset the module via the opto-isolated reset signal. In addition you can remove the XP21 jumper to prevent switching to the BIOS backup.

After the module reboot, the optimal (factory default) BIOS Setup settings can be loaded. If necessary, enter the BIOS Setup, change the necessary parameters, save and exit (paragraph 5.7 Exit).

7. Make sure the module is booted from the main BIOS copy:
a. The jumper XP21 is installed while the XP26 jumper is removed. When booting up, the WDT2 watchdog timer must not be activated (paragraph **4.3.15.2 WDT2 watchdog timer**). Make sure that WDT2 has not been triggered, which can be verified by the LED connected to the XP3 connector (paragraph **4.3.21 LED indication**). You can also check the date and version of the BIOS when going through the POST procedure and in the BIOS Setup menu (Section **5 Basic Input/Output System (BIOS)**).

b. XP21 jumper is removed or both XP21 and XP26 jumpers are installed at the same time. The module always boots from the master copy only. If the module boots, the upgrade is successful.

If the module boots from the main BIOS copy, the upgrade was successful.
If the BIOS backup copy is damaged and the module fails to boot from the backup copy or if the WDT2 watchdog timer occasionally triggers (the XP21 jumper is installed), in this case to restore the BIOS backup copy the module must be sent for repairs with indication of the reason “BIOS backup copy is damaged”.

4.3.16.4.2 BIOS update for module versions 4.x

The main BIOS copy is stored in the FLASH memory integrated into Vortex86DX SoC and connected to the SPI interface.

When updating the BIOS using the integrated console I/O (par.**5.2.3 Remote Access Configuration** (Configuration of Console I/O settings), note that after updating the image and reboot the optimal (factory) BIOS Setup settings will be loaded. If the module is rebooted from the

upgraded to the previous BIOS version, the optimal (factory) BIOS Setup settings will also be loaded. In both cases, the console I/O settings will be changed to the factory settings (Redirection After BIOS POST mode = “Boot Loader”). Therefore, if you want to use the integrated BIOS, you must enter BIOS Setup each time you boot up the module during the BIOS update procedure and set the required settings for the console I/O and BIOS as a whole. It is allowed to use the console I/O by means of the OS so that you don't have to change the BIOS Setup settings every time, which will significantly simplify the BIOS update procedure.

To update the main BIOS copy you need to perform the following steps:

1. Copy the SPIFLASH folder from the relevant section of the FTP server to the module's boot disk. Place the updated BIOS image (for example, c307v310.bin file) in the copied folder.

2. Switch on the CPC307 module and boot into normal mode with the main BIOS copy under FreeDOS.

3. Run the BIOS backup copy update program from the SPIFLASH folder with the “u” key and specify the updated BIOS image:

C:\SPIFLASH\spiflash.exe u c307v311.bin

Attention!
It is not allowed to power off the module or perform any other actions interrupting program operation until SPIFLASH is finished. In a situation where BIOS installation is improperly interrupted, the module will become inoperable. In such a situation, the module must be sent for repairs with the indication of the reason as “Main BIOS copy is damaged” (this case is not covered by the warranty).

If the update is successful, the program will display the following messages:
SPIFLASH 1.11 (May 21 2008)
(C) Copyright 2007 DMP Electronics Inc.
CPU name = Vortex86DX
SPI base address = fc00
send RDID cmd
Device ID=c2 20 15
Flash type = MX25L1605, ok
Update flash rom data from c307v311.bin:
ADDR : 40000/40000
189 blank data block(s) skipped
Ok

4. After the module reboot, the optimal (factory default) BIOS Setup settings can be loaded. If necessary, enter the BIOS Setup, change the necessary parameters, save and exit (paragraph 5.7 Exit).

5. If the module boots, the BIOS copy is updated successfully.

4.3.16.5 Hardware reset of BIOS settings

In modules version 4.x it is possible to reset BIOS settings to optimum (factory) values using the hardware method. In order to do so, it is required:
1. To install the XP27 jumper and turn on the module power. The XP3 LED indication will imply that the XP27 jumper is installed properly (see paragraph **4.3.22 LED indication**).
2. Both XP3 LED indication and the HL1-2 LEDs (blinking with a period of about 0.2 seconds) will imply that the settings are reset. At the same time, the module is not booted.

3. Turn the module power off and remove the XP27 jumper. The settings are reset to optimal values.

4.3.17 Connecting power supply to the module

The +5 V power supply circuit combines the homonymous pins of the XS1 (PCI-104), XS2 (PC-104), and XP22 (additional power supply connector) connectors and is intended for supplying power to the module.

Attention!

When using PC/104 and PC/104+ expansion modules with total power consumption higher than 4W, it is not allowed to power the entire stack through the XP22 connector of the CPC307 module. In this case, you should use the PC/104 sources that allow the stack to be powered via the PC/104 connector.

When a PC/104 or PC/104-plus power supply source is installed, power is supplied to the module via the expansion connector pins.
When using the module independently or without a power supply source in the PC/104 stack, the power can be supplied to the module via an additional XP22 power connector (angled, single-row 4-pin connector with a pitch of 2.5 mm).

The pin assignment of the XP22 power connector is shown in Table 4.28.
An AMP 4-171826-4 connector is installed on the module.

The recommended mating part is AMP 4-171822-4 and AMP 170262-1 set of contacts.

Table 4.28. Pin assignment of the XP22 additional power supply connector

Pin	Signal
1	+5 B
2	GND
3	GND
4	–

To ensure stable operation of the module (not including additional external devices), the external power supply source must provide at least 1 A (+5 V) current consumption.

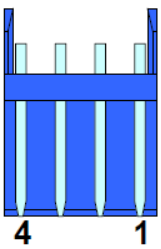


Figure 4.31. Numbering of XP22 connector pins

For muddle versions 4x., the DC/DC converter was upgraded, the “Overvoltage, Overcurrent, Reverse Polarity Protection Circiutry”, “5V Protected” protection nodes were added to prevent module failure due to overvoltage up to +24 V, reverse polarity voltages up to -24 V and short-circuits.

4.3.18 Module power supply voltage supervisor

When the +5V voltage is supplied, the ADM706T supervisor generates a module reset signal of 0.200 seconds duration (the “Powergood” signal will be set by inactive level “0”), provided that the supply voltage exceeds +3.08V. If the +5V voltage drops down to +4.45V during operation, a PFO# (Power Fail Output) signal is generated by the ADM706T supervisor. This signal can be switched to line 0 of GPIO1 port and/or to the IOCHK# (NMI) line of the ISA bus by setting the corresponding jumpers on the XP25 connector pins. When the supply voltage drops down to +3.08 V, a hardware processor reset signal will be generated (the Powergood signal will be set by inactive level "0") until the supply voltage returns to the level above +3.08 V.
See also paragraph **4.3.20 Configuration jumpers** and paragraph **4.3.19 GPIO Ports**.
The opto-isolated reset/interrupt signal (circuit Ext_RST_IRQ# in Figure 4.32) is described in more detail in paragraph **4.3.7 Opto-isolated reset/interrupt**.

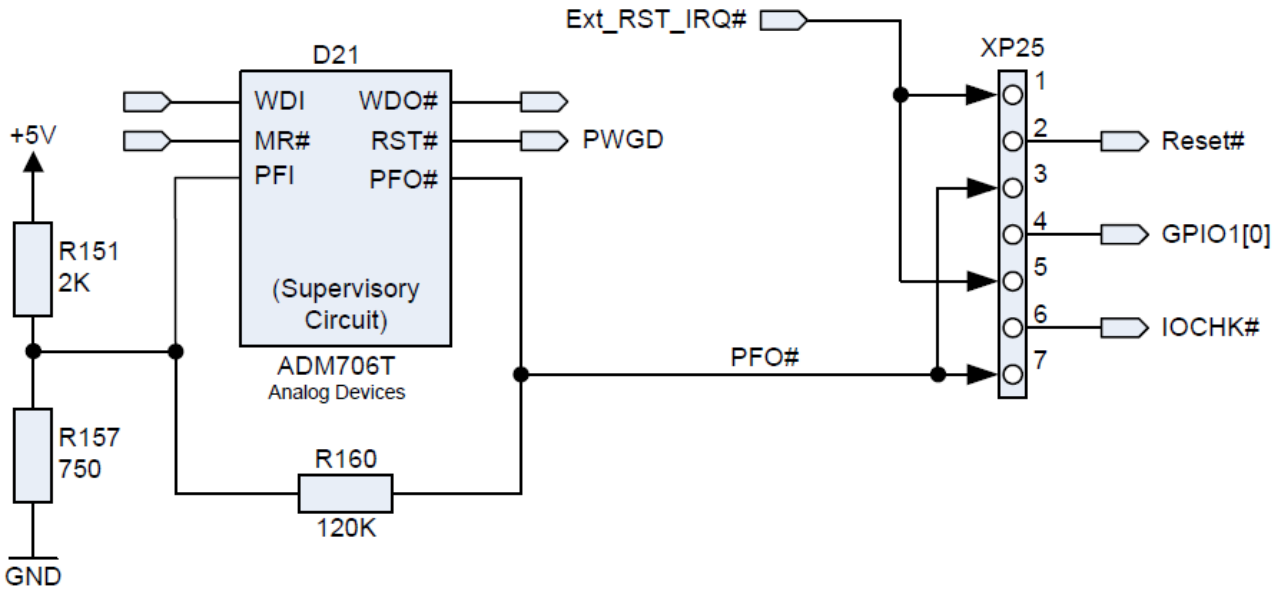


Figure 4.32. Diagram of the module's power supply voltage supervisor

4.3.19 GPIO ports

The Vortex86DX SoC chip has 3 input/output ports - GPIO (General Purpose Input Output), that are accessible to the user through the internal registers of the chip. Each port represents 8 x I/O lines, each of which can be configured as input or output by programming the registers of the corresponding port.
The GPIO ports use two 8-bit registers per port - a data register and a direction register.
Each bit of the data register is matched to a corresponding circuit on the board: bit 0 corresponds to port line 0 (GPIOx0), bit 7 corresponds to port line 7 (GPIOx7), etc.
Each bit of the direction register is matched to a corresponding circuit on the board: bit 0 corresponds to port line 0 (GPIOx0), bit 7 corresponds to port line 7 (GPIOx7), etc.
The GPIO0 port is fully routed to the XP14 connector.
The GPIO1 port is used to control the external watchdog, to enable/disable the soldered ATA Flash disk controller.
The GPIO2 port is used to control COM1, COM2 ports, user LEDs and to read the state of SA1 switch.

Table 4.29 shows the addresses of the GPIO ports registers.
Table 4.30 provides a detailed description of the port lines assignments.

Table 4.29. Description of GPIO ports

	Port 0 (GPIO0)	Port 1 (GPIO1)	Port 2 (GPIO2)	Description
Data register	78h	79h	7Ah	
Direction register	98h	99h	9Ah	0: The line is an input 1: The line is an output

Table 4.30. Description of GPIO ports

I/O port line	I/O line direction	Description
GPIO00 – GPIO07	Configurable by the user	The lines are routed to the XP14 connector
GPIO1[0]	Input	External opto-isolated interrupt line input or input undervoltage signal. 0 - interrupt signal is active, 1 - interrupt signal not active
GPIO1[1]	Output	Resetting the WDT2 watchdog timer. Changing the line status causes the watchdog to reset.
GPIO1[2]	Output	Switching on the WDT2 watchdog timer. 0 – OFF, 1 – ON
GPIO1[3]	Input	Not used
GPIO1[4]	Input	Watchdog state. 0 - was not triggered, 1 – was triggered.
GPIO1[5]	Output	Boot control from external BIOS. 0 - unlock main BIOS chip, 1 - block main BIOS chip. **(Hardware-controlled, changing port value is prohibited)**
GPIO1[6]	Input	Defining module type: 0 – CPC307-02/03, 1 – CPC307-04
GPIO1[7]	Output	Enabling the ATA Flash disk controller. Controlled by BIOS program. 0 - enabled, 1 - disabled. (Hardware-controlled. Changing port value is prohibited)
GPIO2[0]	Output	Switching the operating mode of the COM1 port. GPIO2[0,1]
GPIO2[1]	Output	0x –RS-232 mode, 10 – RS-422 mode, 11 – RS-485 mode.
GPIO2[2]	Output	Switching the operating mode of the COM2 port. GPIO2[2,3]
GPIO2[3]	Output	0x – RS-232 mode, 10 –RS-422 mode, 11 – RS-485 mode.

I/O port line	I/O line direction	Description
GPIO2[4]	Output	Control of HL1 LED. 0 – disabled, 1 – enabled
GPIO2[5]	Output	Control of HL2 LED. 0 – disabled, 1 – enabled
GPIO2[6]	Input	State of the switch 1 of the SA1 switch unit. 0 - switch in “ON” position, 1 - switch in “OFF” position
GPIO2[7]	Input	State of the switch 2 of the SA1 switch unit. 0 - switch in “ON” position, 1 - switch in “OFF” position

Attention!

The +5 V power supply circuit combines homonymous contacts of the XS1 (PCI-104), XS2 (PC-104), and XP22 (additional power connector) connectors and is designed for module's power supply. The +5 V power supply outputs are protected by a 0.5 A fuse. For connected external modules, the recommended current consumption value is not more than 0.4 A. It is not recommended to connect power from interface connectors to more than one external module in order not to overload the power supply circuits of the CPU module.

GPIO0 port lines are routed to the XP14 connector (IDC2-10, 2-row male connector with a pitch of 2 mm).
Pin assignment of the XP14 connector is shown in Table 4.31.
The module has a Leotronics 2073-3102 connector.
The recommended mating part is Leotronics 2039-3101 (ribbon cable press-on socket).

Table 4.31. Pin assignment of the XP14 connector for GPIO0 port

Pin	Signal	Pin	Signal
1	GPIO00	2	GPIO01
3	GPIO02	4	GPIO03
5	GPIO04 /I2C1_SCL	6	GPIO05 /I2C1_SDA
7	GPIO06 /I2C0_SCL	8	GPIO07 /I2C0_SDA
9	GND	10	+5 V

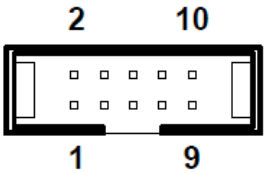


Figure 4.33. Numbering pins of the XP14 connector

4.3.20 Configuration jumpers

Table 4.32. Description of setting the jumpers to the XP4 connector

Jumper state	Function
1 - 2	When the jumper is set, the high-speed mode of the CAN1 interface driver is activated (for speeds higher than 250 Kb/s). When the jumper is removed, the CAN1 interface driver operates in a mode with a reduced level of emitted electromagnetic interference due to a lower steepness of the signal edges.
3 - 4 (for module versions older than 4.x) 3 - 4 and 5 - 6 (for module versions 4.x)	When the jumper is set, a 120 ohm terminating resistor is connected to the CAN1 line.

Table 4.33. Description of setting the jumpers to the XP8 connector

Jumper state	Function
1 - 2	When the jumper is set, the high-speed mode of the CAN2 interface driver is activated (for speeds higher than 250 Kb/s). When the jumper is removed, the CAN2 interface driver operates in a mode with a reduced level of emitted electromagnetic interference due to a lower steepness of the signal edges.
3 - 4 (for module versions older than 4.x) 3 - 4 and 5 - 6 (for module versions 4.x)	When the jumper is set, a 120 ohm terminating resistor is connected to the CAN2 line.

Table 4.34. Description of setting the jumpers to the XP15 connector (for module versions lower than than 4.x)

Jumper state	Function
1 - 2	If the jumper is set on the TX+/TX- line of the COM5 interface, a 120 ohm terminating resistor is connected.
3 - 4	If the jumper is set on the RX+/RX- line of the COM5 interface, a 120 ohm terminating resistor is connected.

Table 4.35. Description of setting the jumpers to the XP15 connector for module versions 4.x

Jumper state	Function
1 - 2	The +TX signal is pulled up through a 680 Ohm resistor to the +5V supply voltage to generate a 200 mV offset on Y/Z lines.
3 - 4	The -TX signal is pulled up through a 680 Ohm to the GND for generation of a -200 mV offset on Y/Z lines.
5 - 6	When the jumper is set to the RX + / RX- line of the COM5 interface (in the RS-422/485 mode), the 120 Ohm terminating resistor is connected.
1 - 2 and 3 - 4	When the jumper is set to TX+/TX- line of COM5 interface (in RS-422/485 mode), 120 Ohm terminating resistor is connected.

Table 4.36. Description of setting the jumpers to the XP18 connector for module versions older than 4.x

Jumper state	Function
1 - 2	When the jumper is set to TX+/TX- line of COM1 interface (in RS-422/485 mode), a 120 Ohm terminating resistor is connected.
3 - 4	When the jumper is set to RX+/RX- line of COM1 interface (in RS-422/485 mode), a 120 Ohm terminating resistor is connected.
5 - 6	When the jumper is set to TX+/TX- line of COM2 interface (in RS-422/485 mode), 120 Ohm terminating resistor is connected.
7 - 8	When the jumper is set to RX+/RX- line of COM2 interface (in RS-422/485 mode), a 120 Ohm terminating resistor is connected.

Table 4.37. Description of setting the jumpers to the XP18 connector for module versions 4.x

Jumper state	Function
1 - 2 and 9 - 10	When the jumper is set to TX+/TX- line of COM1 port (in RS-422/485 mode), a 120 Ohm terminating resistor is connected.
3 - 4	When the jumper is set to the RX+/RX- line of COM1 port (in the RS-422/485 mode), a 120 Ohm terminating resistor is connected.
1 - 2	Signal +TX of COM1 port is pulled up through the 680 Ohm resistor to a supply voltage of +5V to generate the +200 mV offset on Y/Z lines.
9 - 10	Signal -TX of COM1 port is pulled up through the 680 Ohm resistor to ground GND to generate the -200 mV offset on the Y/Z lines.
5 - 6 and 11 - 12	When the jumper is set to TX+/TX- line of COM2 port (in RS-422/485 mode), a 120 Ohm terminating resistor is connected.
7 - 8	When the jumper is set to RX+/RX- line of COM2 port (in RS-422/485 mode), a 120 Ohm terminating resistor is connected.
5 - 6	Signal +TX of COM2 port is pulled up through the 680 Ohm resistor to a supply voltage of +5V to generate the +200 mV offset on the Y/Z lines
11 - 12	Signal -TX of COM2 port is pulled up through the 680 Ohm resistor to GND to generate the -200 mV offset on the Y/Z lines

Table 4.38 Description of setting the jumpers to the XP20 connector for module versions lower than 4.x

Jumper state	Function
1 - 2	When the jumper is set to the TX+/TX- line of the COM6 interface, a 120 Ohm terminating resistor is connected.
3 - 4	When the jumper is set to the RX+/RX- line of the COM6 interface, a 120 Ohm terminating resistor is connected.

Table 4.39 Description of setting the jumpers to the XP20 connector for module versions 4.x

Jumper state	Function
1 - 2	Signal +TX is pulled up through the 680 Ohm resistor to the +5V power supply voltage to generate a 200 mV offset on the Y/Z lines.
3 - 4	Signal –TX is pulled up through a 680 Ohm resistor to GND to generate the -200 mV offset on the Y/Z lines.
5 - 6	When the jumper is set to the RX + / RX- line of COM6 interface (in the RS-422/485 mode), a 120 Ohm terminating resistor is connected.
1 - 2 and 3 - 4	When the jumper is set to the TX+/TX- line of COM6 interface (in the RS-422/485 mode), a 120 Ohm terminating resistor is connected.

Table 4.40. Description of setting the jumpers to the XP24 connector

Jumper state	Function
1 - 2	Operating mode of the soldered ATA Flash disk controller. The jumper is installed - Master mode. The jumper is removed - Slave mode.
2 - 3	When the jumper is set, the ATA Flash disk controller is disconnected from the IDE bus, which allows you to connect up to 2 x external IDE devices (in module versions older than 4.x this function is not supported, this configuration is unacceptable, please see Section 8)

Table 4.41. Description of setting the jumpers to the XP25 connector

Jumper state	Function
1 - 2	When the jumper is set, the external opto-isolated signal performs the module reset function. (External RESET#)
2 - 3	When the jumper is set, the +5V power supply voltage drop signal down to the value of ... (PFO#) performs the module reset function. (Power Fail RESET#)
3 - 4	When the jumper is set, the +5 V supply voltage drop signal down to the value of ... (PFO#) is switched to the line of the GPIO1[0] I/O port. (Power Fail GPIO1[0]#)
4 - 5	When the jumper is set, the external opto-isolated signal is switched to the line of GPIO1[0] I/O port. (External GPIO1[0]#)
5 - 6	When the jumper is set, the external opto-isolated signal is switched to the IOCHK# line of the ISA bus. (External INTERRUPT#).
6 - 7	When the jumper is set, the +5 V power supply voltage drop signal down to the value of ... (PFO#) is switched to the IOCHK# line of the ISA bus. (Power Fail INTERRUPT#)

Table 4.42. Description of setting the jumpers to the XP21 connector (for module versions lower than 4.x)

Jumper state	Function
1 - 2	If the jumper is set, triggering the external watchdog timer of the module will make it restart from the BIOS backup copy. If the jumper is removed, triggering the external watchdog timer will make the module to reboot from the main BIOS copy.

Table 4.43. Description of setting the jumpers to the XP26 connector

Jumper state	Function
1 - 2	**For module versions older than 4.x:** When the jumper is installed, the external watchdog in the ADM706T power supply supervisor chip is disabled. When the jumper is removed, the external watchdog in the ADM706T power supply supervisor chip is enabled. **For module versions 4.x and higher:** When the jumper is installed, the external watchdog in the ADM706T power supply supervisor chip is enabled. When the jumper is removed, the external watchdog timer in the ADM706T power supply supervisor chip is disabled.

Table 4.44. Description of setting the jumpers to the XP27 connector

Jumper state	Function
1 - 2	**For module versions lower than 4.x:** Functions when the jumper is installed: When the jumper is installed, triggering the external watchdog timer will make the module to restart from the main BIOS copy if the XP21 jumper is installed. When the jumper is removed, triggering the external watchdog timer will make the module to restart from the backup BIOS copy if the XP21 jumper is installed. Function when an external normally open button (primary) is connected: control of the LED connected to the XP3, pins 5-6. When the pins are shorted, the LED will be turned off if it is turned on after an external watchdog timer was triggered. **For module versions 4.x and higher:** If the jumper is installed, after supplying power to the module, the BIOS settings will be reset to factory defaults/optimal. In this case the module will not boot. After removing the jumper, the module will start with the factory BIOS settings.

4.3.21 LEDs

There are 3 x LEDs on the module (HL1 to HL2). Assignment of the module LEDs is shown in Table 4.45.

Table 4.45. Assignment of module LEDs

LED	Color	Function
HL3	Yellow	Indication of +5 V supply voltage
HL1	Green	User LED. Controlled by GPIO2[4] line
HL2	Green	User LED. Controlled by GPIO2[5] line

The module has an XP3 for connecting external LED indication.
The pin assignment is shown in Table 4.46. Functional diagram of signal output for indication is shown in Figure 4.34.

Table 4.46. Pin assignment of the XP3 connector

Pin	Circuit current	Function
1 – 2	R=510, U=+5V	Ethernet Link ACT
3 – 4	R=510, U=+5V	Ethernet Duplex
5 – 6	R=330, U=+1.8V	WDO ACT for module versions lower than 4.x BIOS DEFAULT for module versions 4.x
7 – 8	R=330, U=+3.3V	CPU_RESET
9 – 10	R=510, U=+5V	IDE ACT
11 – 12	R=330, U=+3.3V	USER1 (GPIO2_5)
13 – 14	R=330, U=+3.3V	USER0 (GPIO2_4)

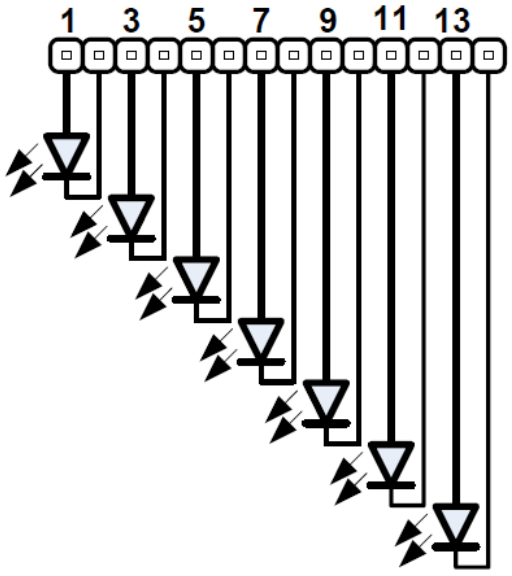


Figure 4.34. Connection of LEDs to the XP3

4.3.22 Specific features of console redirect module operation

BIOS has a console redirect module, designed to work with the board in the terminal mode. To continue the module's operation after OS startup you must enable BIOS Setup option “Redirection After BIOS → Always”.
If there is no installed video adapter card, the video buffer is generated by the redirection module and does not use the segment 0xB800. Therefore, the output of software that directly writes to the video memory or uses unsupported Int 0x10 functions is either distorted or does not reach the terminal at all. This peculiarity must be taken into account when writing applications that work in configurations without a video adapter.

List of Int 0x10 functions supported by the redirect module:

- Int 0x10 , AH=0x00 - Set Video Mode
- Int 0x10 , AH=0x01 - Set Cursor Type
- Int 0x10 , AH=0x02 - Set Cursor Position
- Int 0x10 , AH=0x03 - Read Cursor Position
- Int 0x10 , AH=0x06 AL=0 - Clean a block.
- Int 0x10 , AH=0x08 - Read Character And Attribute At Cursor.
- Int 0x10 , AH=0x09 - Write Character And Attribute At Cursor.
- Int 0x10 , AH=0x0A - Write Character At Current Cursor.
- Int 0x10 , AH=0x0E - Write Text In Teletype Mode.
- Int 0x10 , AH=0x0F - Get Current Video State.
- Int 0x10 , AH=0x13 - Write String.

A list of Int 0x10 functions that are **NOT supported** by the redirect module:

- Int 0x10, AH=0x04 - Read Light Pen.
- Int 0x10, AH=0x05 - Select Active Display
- Int 0x10, AH=0x06 - Scroll Active Page Up.
- Int 0x10, AH=0x07 - Scroll Active Page Down.
- Int 0x10, AH=0x0B - Set Color Palette.
- Int 0x10, AH=0x0C - Write Graphics Pixel At Coordinate.
- Int 0x10, AH=0x0D - Read Graphics Pixel At Coordinate.
- Int 0x10, AH=0x10 - Set/Get Palette Registers.
- Int 0x10, AH=0x11 - Character Generator Routine.
- Int 0x10, AH=0x12 - Video Subsystem Configuration.

5 Basic Input/Output System (BIOS)

To enter BIOS Setup, at system boot during the POST (Power On Self Test) procedure, press the “DEL” key on your keyboard or the “F4” key on the console PC keyboard (if the “Console Redirect” option is enabled). An example of the screen during the POST procedure is shown in Figure 5.1.

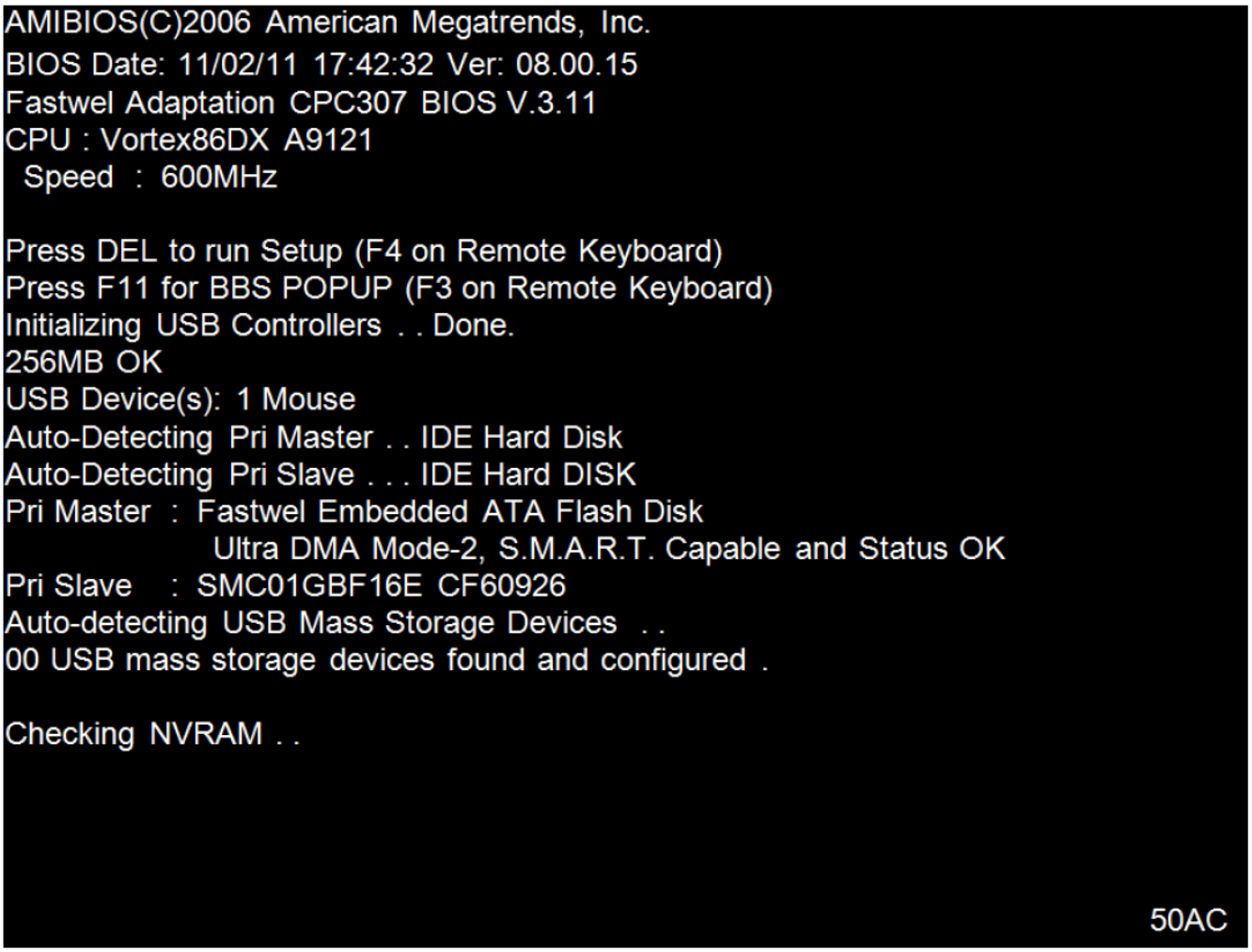


Figure 5.1. Screen during the module boot (POST)

The BIOS Setup Utility allows you to change BIOS (Basic Input Output System) parameters and manage the special modes of the module. This program uses a menu system to make changes and to enable or disable special functions.
The information fields (highlighted in gray) are used to display additional information about the module and/or module settings and cannot be modified by the user.
When describing the menu items, the default values are underlined. Information fields are italicized. Setting incorrect values may lead to system malfunctions.
Depending on the BIOS version, the number and values of menu items may differ from the description of the v.3.11 BIOS version for the CPC307 v.3.1 modules below.
To get a hint about the function keys used for easy navigation through the menu items, press the F1 key after entering the BIOS Setup.
The notices on the BIOS Setup screenshots below are conventional; the exact values are given in the tables.

5.1 Main

This tab contains a description of the BIOS version, the installed CPU and RAM. There are also two items responsible for setting the current time and date. The screen view of the “Main” menu is shown in Figure 5.2, the description of the items is given in Table 5.1.

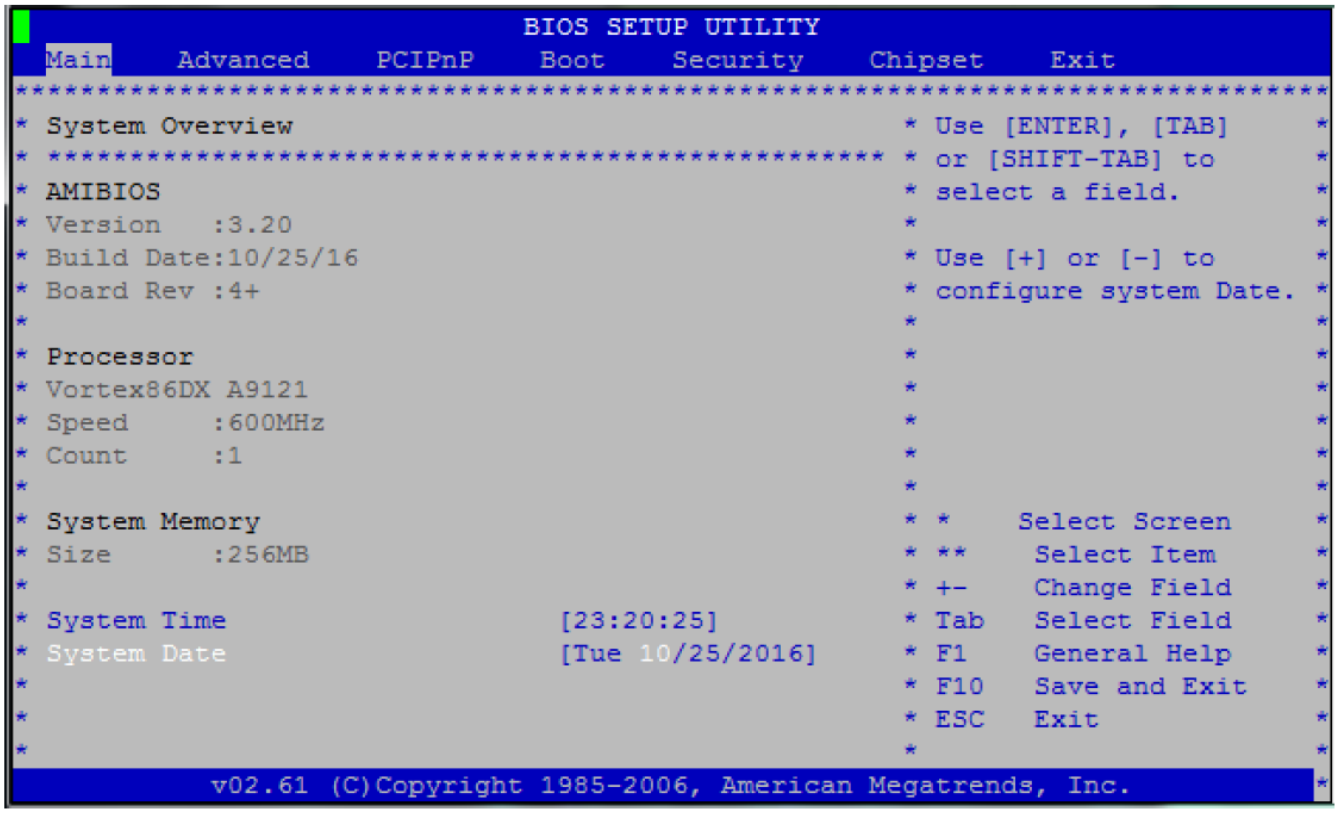


Figure 5.2. Screen of the “Main” menu

Table 5.1. Description of the “Main” menu

Menu item	Purpose
AMIBIOS	BIOS version information: *Version* – current version of the BIOS kernel, 08.00.14 – without SMI support, 08.00.15 – with SMI support *Build Date* – a calendar date on which a BIOS version is built *Board Rev* – the current version of the module: *“std”* – module versions lower than 4.x, “4+” – module versions 4.x
Processor	Information about the processor installed on the module: *Vortex86DX A9121* – version of the processor Vortex86DX rev.D *Speed* – processor clock frequency *Count* – number of processors in the system, always 1
System Memory	Information about the DDR2 SDRAM installed on the module: *Size* – RAM size, fixed, 256 MB
System Time	Current time in the format [hour/minute/sec]
System Date	Current date in the format [month/day/year]

5.2 Advanced

This menu tab contains items responsible for operation of the soldered ATA Flash Disk controller, processor cache, IDE bus, console I/O and USB devices. The screen view of the Advanced menu is shown in Figure 5.3, the description of the items is given in Table 5.2.

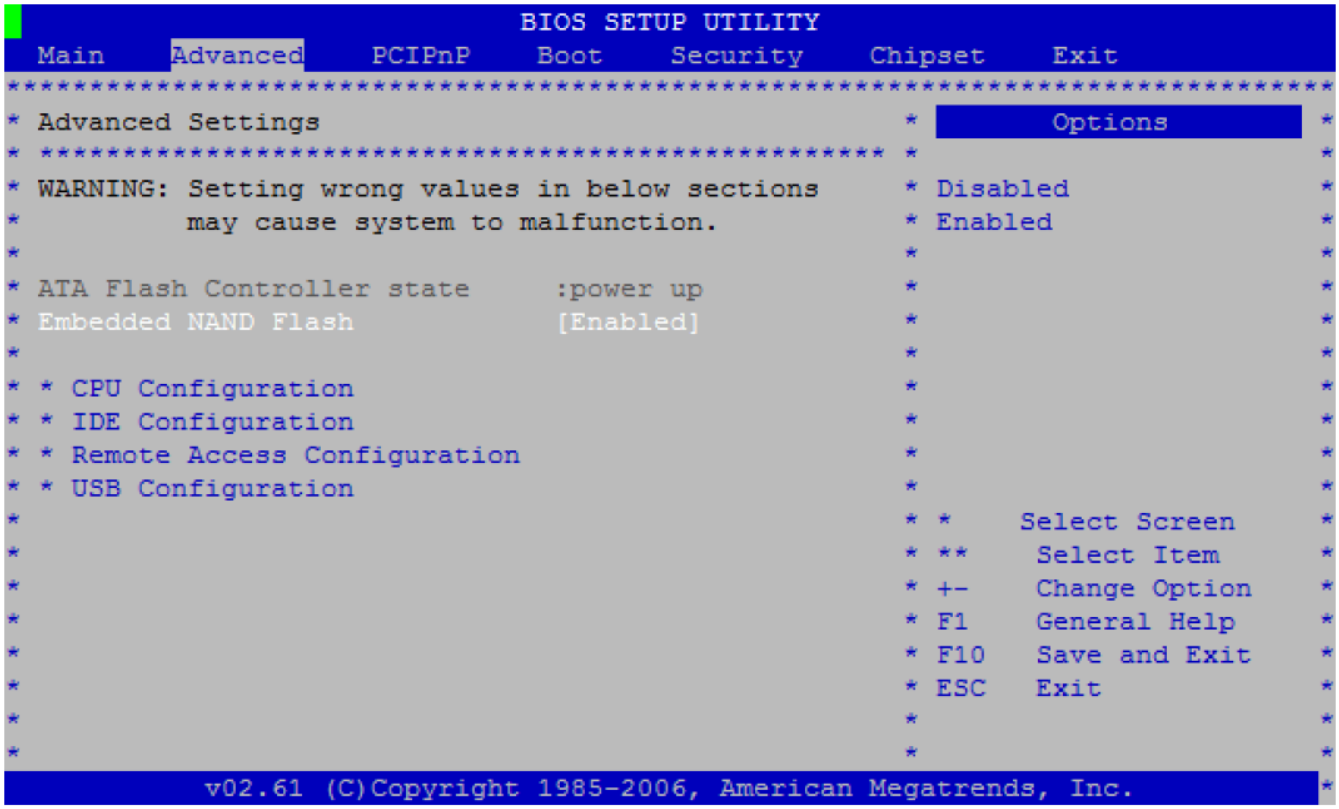


Figure 5.3. Screen of the “Advanced” menu

Table 5.2. Description of "Advanced" menu

Menu item	Purpose	
ATA Flash Controller state	NAND controller status	
	“power up”	NAND controller is hardware switched on
	“power down”	NAND controller is hardware switched off
	“unknown or SD”	No NAND controller (version CPC307-04 or version 3.x)
Embedded NAND Flash 1), 2)	The soldered ATA Flash Disk controller is enabled	
	[Enabled]	Operations is enabled
	[Disabled]	Operation is disabled
CPU Configuration (submenu)	CPU manufacturer information is shown here, as well as options to control the operation of the embedded cache memory in the CPU	
IDE Configuration (submenu)	Controls the operation of devices on an IDE bus	

Remote Access Configuration (submenu)	Console I/O settings
USB Configuration (submenu)	USB Port Settings. These settings apply to all 4 USB ports

Notes:

1) Version 3.x modules do not have the "Embedded NAND Flash" feature;

2) The CPC307-04 version has no "Embedded NAND Flash" function.

5.2.1 CPU Configuration

The “CPU Configuration” menu screen is shown in Figure 5.4, description of the items is given in Table 5.3.

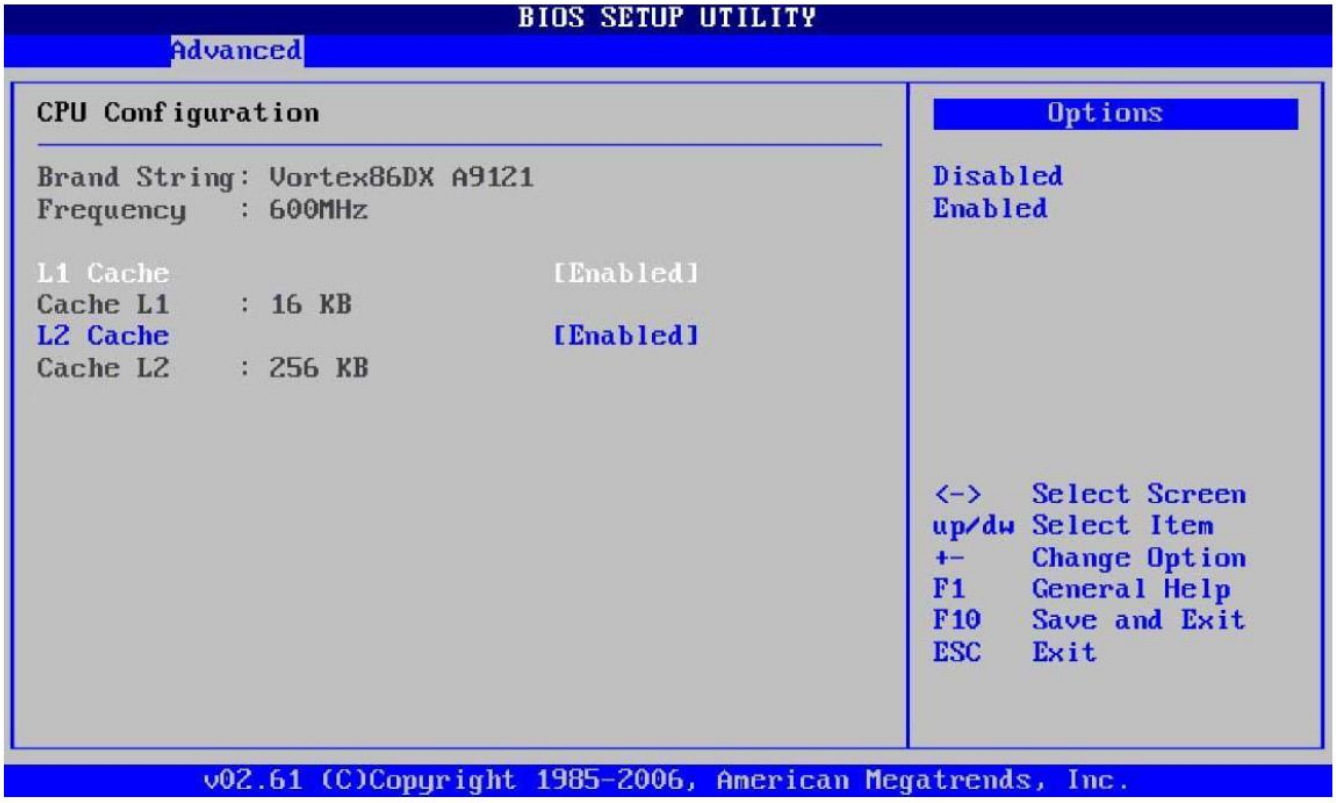


Figure 5.4. Screen of the “CPU Configuration” menu

Table 5.3. Description of the “CPU Configuration” menu

Menu item	Purpose	
CPU Configuration	Information on the module and CPU: *Brand String* – CPU identifier, *Frequency* – CPU clock frequency.	
L1 Cache	[Enabled]	Level 1 cache is enabled
	[Disabled]	Level 1 cache is disabled
L2 Cache	[Enabled]	Level 2 cache is enabled
	[Disabled]	Level 1 cache is disabled

5.2.2 IDE Configuration

The “IDE Configuration” menu is shown in Figure 5.5, the description of the items is given in Table 5.4. For more information on the IDE controller operation, please refer to the description of the AT Attachment with Packet Interface - 6 (ATA/ATAPI-6) standard.

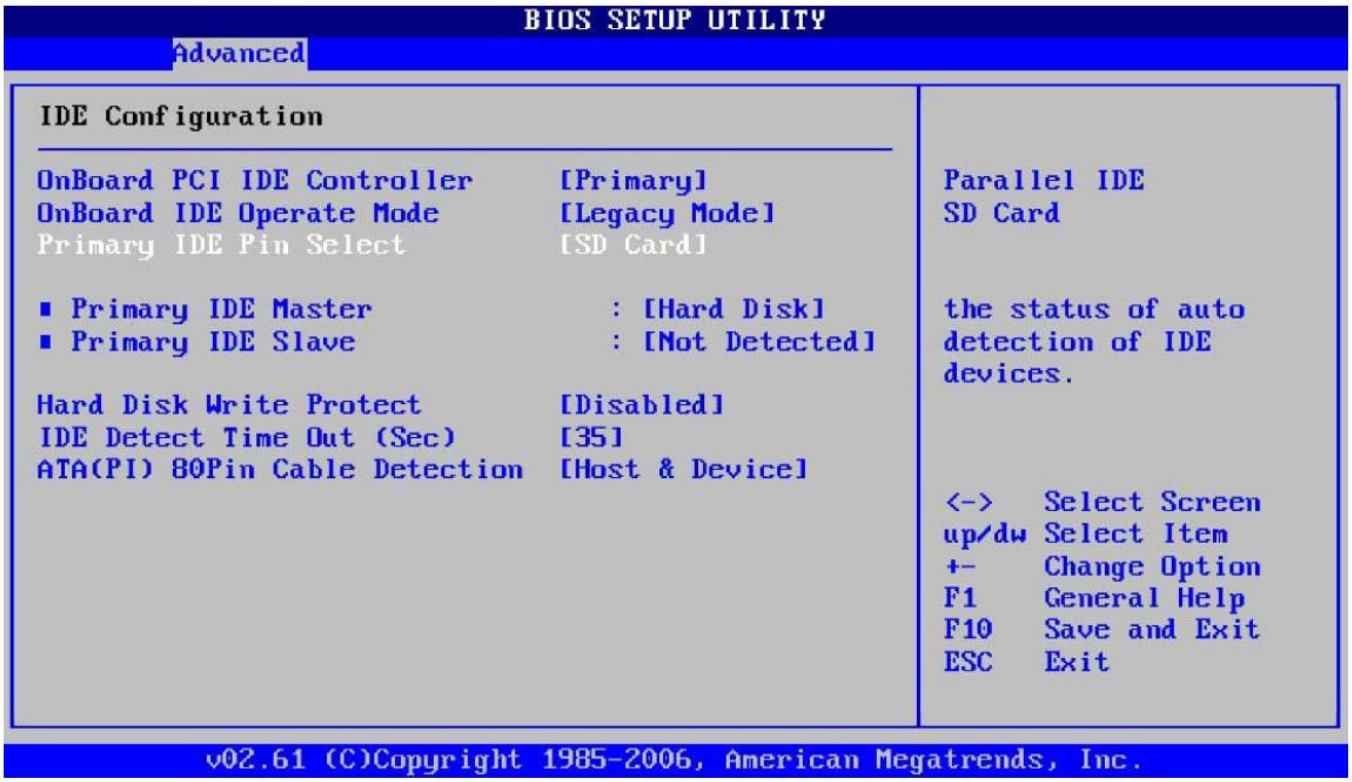


Figure 5.5. Screen of the “IDE Configuration” menu

Table 5.4. Description of the “IDE Configuration” menu

Menu item	Purpose	
Onboard PCI IDE Controller	Controls operation of the integrated IDE bus controller	
	[Primary]	Operation is enabled
	[Disabled]	Operation is disabled
Onboard IDE Operate Mode	Controls operation of the integrated IDE bus controller	
	[Legacy Mode]	IDE controller operation in Legacy mode
	[Native Mode]	IDE controller operation in Native mode
Primary IDE Pin Select *(item is present only for the module CPC307-04)*	Controls operation of the integrated IDE bus controller.	
	[SD Card]	Operation of the IDE controller in SD card support mode
	[Parallel IDE]	Operation of the IDE controller in IDE device support mode
Primary IDE Master (submenu)	This menu item contains information about the connected IDE device operating in Master mode (Figure 5.5, Table 5.3).	
Primary IDE Slave (submenu)	This item contains information about the connected IDE device operating in Slave mode. The structure of the menu is completely identical to that of the Primary IDE Master menu (Figure 5.5, Table 5.3).	

Hard Disk Write Protect	Access denial to writing to IDE devices	
	[Enabled]	Enable denial
	[Disabled]	Disable denial
IDE Detect Time Out (Sec)	Time limit for ATA/ATAPI device detection, in sec. The following values are available:	
	[0], [5], [10], [15], [20], [25], [30] ,[35]	
ATA(PI) 80Pin Cable Detection	Selects the way which is used for detection of the 80-core ATA(PI) cable	
	[Host & Device]	Detection by system and IDE devices
	[Host]	Detection by system only
	[Device]	Detection by IDE devices only. In Native mode of IDE controller this may lead to data loss on the integrated ATA Flash disk

5.2.2.1 Primary IDE Master

The “Primary IDE Master” menu screen is shown in Figure 5. 6., the description of the items is given in Table 5.5. The “IDE Primary Slave” menu is completely identical to the "Primary IDE Master” menu.

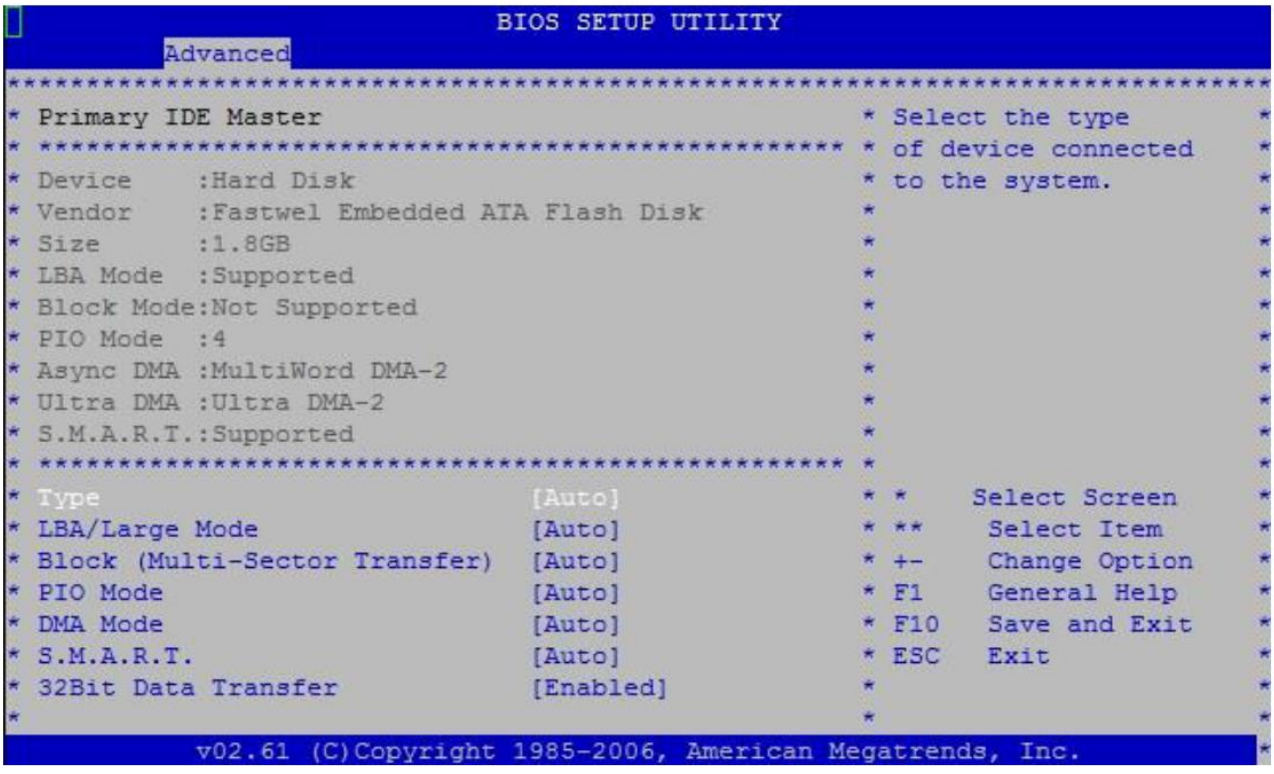


Figure 5.6. Screen of the “Primary IDE Master” menu

Table 5.5 Description of the “Primary IDE Master” menu

Menu item	Purpose	
Type	Type of the device connected to this IDE channel	
	[Not Installed]	Search for the connected devices is disabled
	[Auto]	Automatic detection of the connected device type
	[CD/DVD]	Detect the device type as CD/DVD drive

	[ARMD]	Detect the connected device as an ATAPI Removable Media Device (ZIP, LS-120)
LBA/Large Mode	Addressing type of the device connected to this IDE channel	
	[Auto]	Automatic detection of LBA Mode support
	[Disabled]	Disabled detection of LBA Mode, Large Mode is used
Block (Multi-Sector	Block communication mode	
Transfer)	[Auto]	This option enables BIOS to automatically detect if the Multi-Sector Transfer mode is supported at this channel. This option enables BIOS to automatically detect the number of sectors per block for data transfers from the disk to memory. Data to/from the device will be transferred by multiple sectors at a time. Default value.
	[Disabled]	This option disables BIOS to use Multi- Sector Transfer mode on the current channel. Data to and from the device will be transferred one sector at a time.
PIO Mode	Programmable I/O mode (PIO)	
	[Auto]	This option allows the BIOS to automatically detect if the device supports PIO mode. It is recommended to use this setting when the supported mode of the connected device cannot be detected.
	[0]	Set the connected device to PIO 0 mode. The data transfer rate in this mode is up to 3.3 MB/sec.
	[1]	Set the connected device to PIO 1 mode. The data transfer rate in this mode is up to 5.2 MB/sec.
	[2]	Set the connected device to PIO 2 mode. The data transfer rate in this mode is up to 8.3 MB/sec.
	[3]	Set the connected device to PIO 3 mode. The data transfer rate in this mode is up to 11.1 MB/sec.
	[4]	Set the connected device to PIO 4 mode. The data transfer rate in this mode is up to 16.6 MB/sec.
DMA Mode	DMA (Direct Memory Access) transfer mode	
	[Auto]	Recommended value for most efficient data transfer. As of BIOS v3.12 only UDMA0 mode is supported.
	[SWDMA0] [SWDMA1] [SWDMA2]	Single Word DMA modes
	[MWDMA0] [MWDMA1] [MWDMA2]	Multi Word DMA modes
	[UDMA0] [UDMA1] [UDMA2]	Ultra DMA modes
S.M.A.R.T.	Smart Monitoring, Analysis, and Reporting Technology	
	[Auto]	The BIOS will automatically detect and support the connected device. It is recommended to use this option if the connected drive cannot be detected and supported.
	[Enabled]	This option allows the BIOS to use the SMART function when dealing with the connected drives.
	[Disabled]	This option disables the BIOS to use the SMART function with the connected drives
32-bit Data Transfer	32-bit data transfer mode	
	[Enabled]	This option enables 32-bit data transfer for the connected device
	[Disabled]	This option disables 32-bit data transfer for the connected device

5.2.3 Remote Access Configuration

The Remote Access Configuration menu screen is shown in Figure 5. 7, the description of the items is given in Table 5. 6.

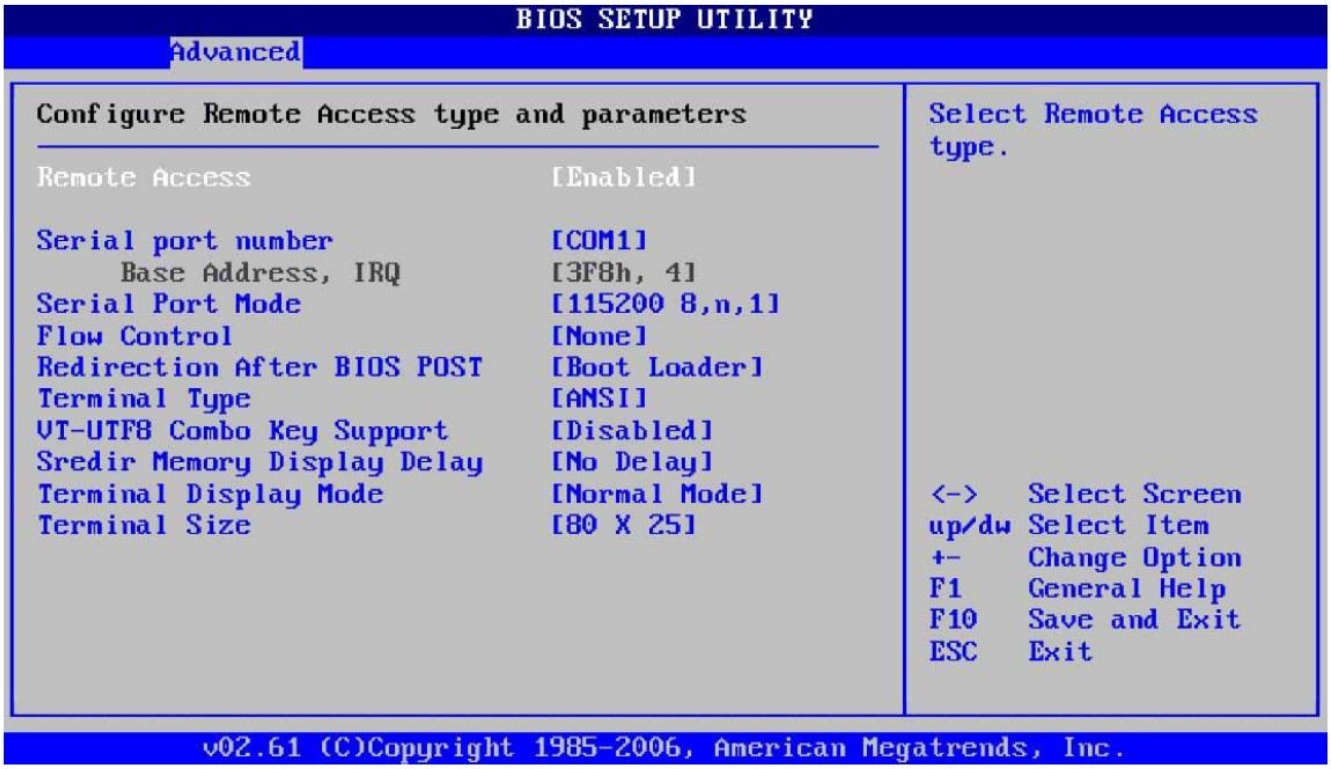


Figure 5.7. Screen of the "Remote Access Configuration" menu

Table 5.6. Description of the "Remote Access Configuration" menu

Menu item	Purpose	
Remote Access	Remote access	
	[Disabled]	Remote access disabled
	[Enabled]	Remote access is enabled, additional options for remote access settings become available.
Serial port number	Selection of a serial port for remote access	
	[COM1]	COM1 port is used as remote access port
	[COM2]	COM2 port is used as remote access port
	[COM3]	COM3 port is used as remote access port
	[COM4]	COM4 port is used as remote access port
Serial port mode	Serial port operation mode	
	[115200 8,n,1],	Baud rate 115.2 kbaud, 8-bit, no parity, 1 stop bit
	[57600 8,n,1],	Baud rate 57.6 kbaud, 8-bit, no parity, 1 stop bit
	[38400 8,n,1],	Baud rate 38.4 kbaud, 8-bit, no parity, 1 stop bit
	[19200 8,n,1],	Baud rate 19.2 kbaud, 8-bit, no parity, 1 stop bit
	[09600 8,n,1],	Baud rate 9.6 kbaud, 8-bit, no parity, 1 stop bit
Flow Control	Flow control for remote access	

	[None]	None
	[Hardware]	CTS/RTS hardware control
	[Software]	XON/XOFF software control
Redirection After BIOS POST	Redirection After BIOS POST	
	[Disabled]	Disable remote access after the BIOS POST procedure
	[Boot Loader]	Remote access is active during BIOS POST and OS boot
	[Always]	Remote access is always active. Some operating systems may not support this option
Terminal Type	Terminal type	
	[ANSI]	ANSI standard
	[VT100]	VT100 standard
	[VT-UTF8]	VT-UTF8 standard
VT-UTF8 Combo Key Support	VT-UTF8 symbols support for ANSI/ME100 terminals	
	[Disabled]	Support is disabled
	[Enabled]	Support is enabled
Sredir Memory Display Delay	Sets the delay after displaying the module's system memory information at a remote PC screen	
	[No Delay]	No delay
	[Delay 1 Sec],	Sets delay for 1 sec.
	[Delay 2 Sec],	Sets delay for 2 sec.
	[Delay 4 Sec]	Sets delay for 4 sec.
Terminal Display Mode	Data transfer mode to the console PC	
	[Normal Mode]	Normal mode
	[Recorder Mode]	Text only
Terminal Size	Number of transmitted symbols and lines	
	[80x24]	80 symbols, 24 lines
	[80x25]	80 symbols, 25 lines

5.2.4 USB Configuration

The “USB Configuration” menu screen is shown in Figure 5.8, the description of the items is given in Table 5.7.

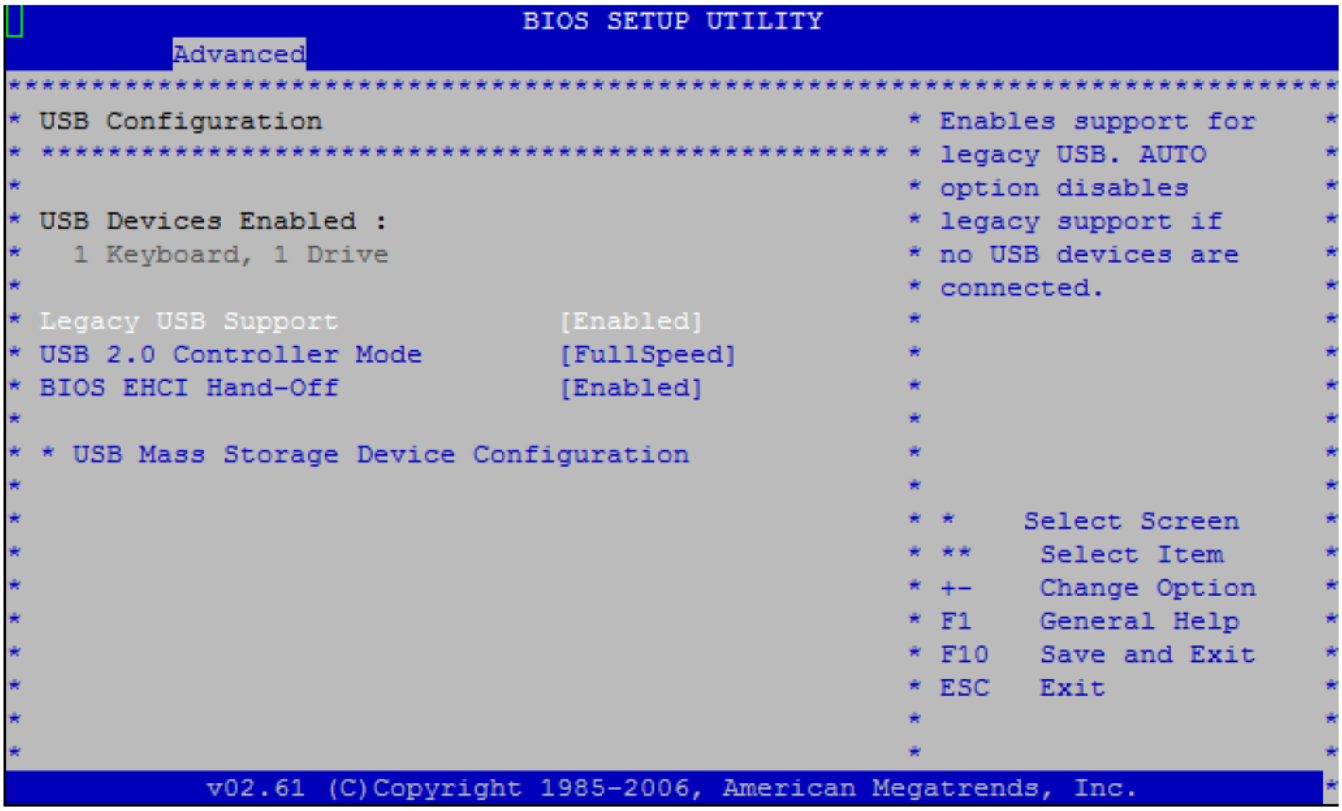


Figure 5.8. Screen of the “USB Configuration” menu

Table 5.7 Description of the “USB Configuration” menu

Menu item	Purpose	
Legacy USB Support	Legacy USB device support management	
	[Disabled]	Support is disabled
	[Enabled]	Support is enabled, recommended value
	[Auto]	Automatic detection
USB 2.0 Controller Mode	Defining the data exchange rate with a USB device	
	[HiSpeed]	Data exchange rate is 25-480 Mb/sec.
	[FullSpeed]	Data exchange rate is 0.5-12 Mb/sec (mode USB 1.0/1.1)
USB EHCI Hand-Off	BIOS support of EHCI (Enhanced Host Controller Interface) control mechanism between the devices	
	[Disabled]	Controlled by operating system
	[Enabled]	Controlled by means of BIOS
USB Mass Storage Device Configuration	Setting the emulation mode of the connected USB storage devices	

5.2.5 USB Mass Storage Device Configuration

The “USB Mass Storage Configuration” menu is shown in Figure 5.9, the description of the items is given in Table 5.8.

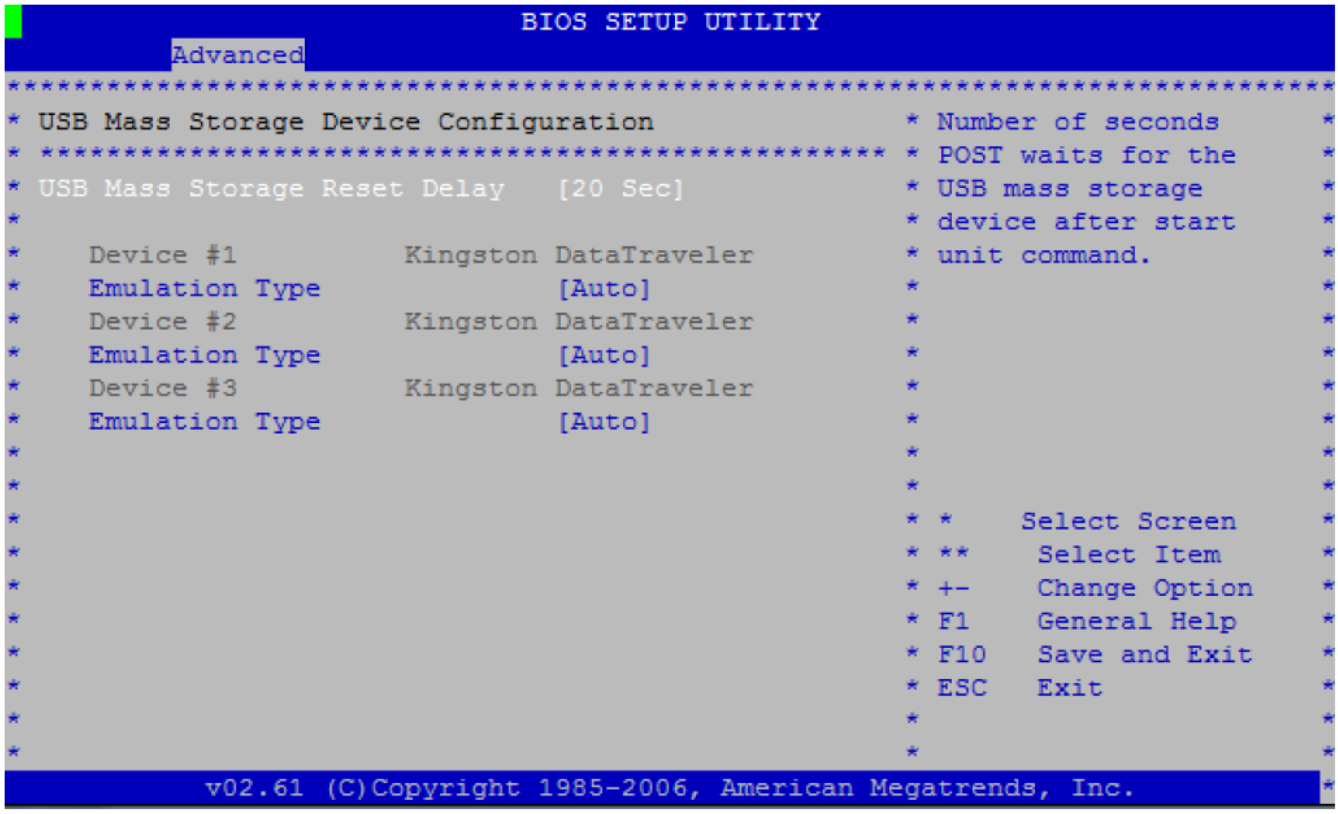


Figure 5.9. Screen of the “USB Mass Storage Device Configuration” menu

Table 5.8. Description of the “USB Mass Storage Device Configuration” menu

Menu item	Purpose	
USB Mass Storage Reset Delay	USB drive detection delay	
	[10 sec]	USB-drive detection delay for 10 sec.
	[20 sec]	USB-drive detection delay for 20 sec.
	[30 sec]	USB-drive detection delay for 30 sec.
	[40 sec]	USB-drive detection delay for 40 sec.
Device #1-4 Emulation Type	Setting the operation mode of USB flash drive port #1-4	
	[Auto]	Automatic detection of emulation mode
	[Floppy]	Floppy disk drive emulation mode
	[Forced FDD]	Forced Floppy disk drive emulation mode
	[Hard Disk]	Hard disk emulation mode
	[CDROM]	CD-ROM emulation mode

5.3 PCIPNP

This tab contains items responsible for PCI and ISA bus operation as well as interrupt switching control. The screen view of the PCIPnP menu is shown in Figure 5.10, the menu description is given in Table 5.9.

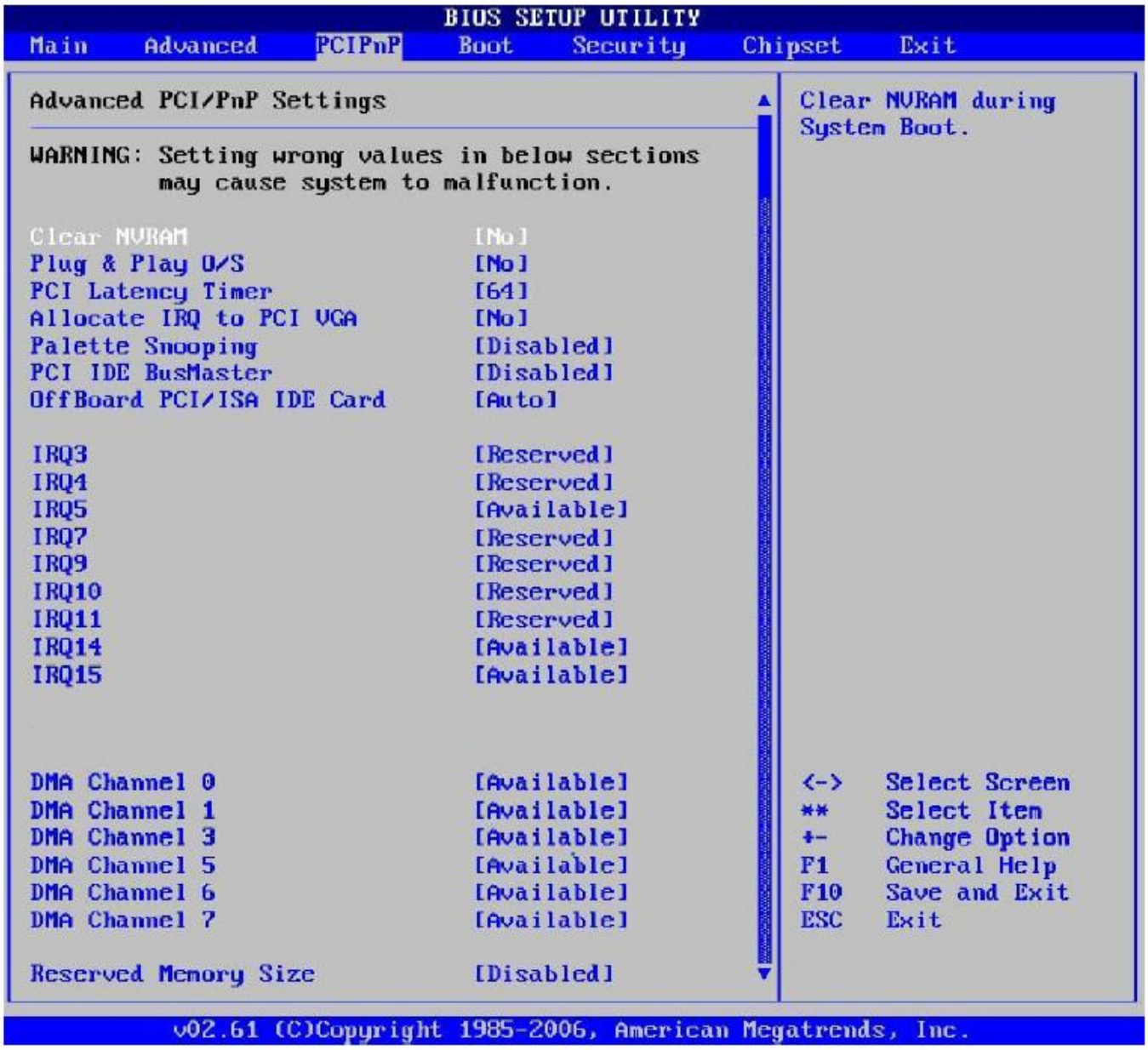


Figure 5.10. Screen of the "PCIPnP" menu

Table 5.9. Description of the "PCIPnP" menu

Menu item	Purpose	
Clear NVRAM	Resetting the PnP parameter table	
	[No]	No changes
	[Yes]	Reset the table after reboot
Plug & Play O/S	PnP-supported operating system installed	

	[No]	No
	[Yes]	Yes
PCI Latency Timer	The maximum number of PCI bus cycles during which the device connected to the bus can keep it busy by transmitting data.	
	[32], [64], [96], [128], [160], [192], [224], [248]	
Allocate IRQ to PCI VGA	Enabling assigning interrupts to PCI bus video card	
	[No]	Do not assign the PCI interrupt to the graphics card
	[Yes]	Assigning PCI interrupt to the graphics card
Palette Snooping	Synchronizing the colors of the graphics card and the image captured by the video I/O card (video editing card).	
	[Disabled]	Function is disabled. Recommended value.
	[Enabled]	Function is enabled.
PCI IDE BusMaster	Enable Bus Mustering PCI mode on IDE bus controller	
	[Disabled]	Disables Bus Mastering mode
	[Enabled]	Enables Bus Mastering mode
OffBoard PCI/ISA IDE Card	External PCI/ISA card selection by IDE bus controller	
	[Auto]	Automatic detection of the presence of PCI/ISA card of IDE bus controller. Recommended value.
	[PCI Slot1], [PCI Slot2], [PCI Slot3], [PCI Slot4], [PCI Slot5], [PCI Slot6]	Specify that an IDE bus controller card is installed in the corresponding PCI slot
IRQ3 IRQ4 IRQ5 IRQ7 IRQ9 IRQ10 IRQ11 IRQ14 IRQ15	Reserved IRQ interrupt for internal Legacy devices of Vortex86DX SoC	
	[Available]	Enabling external PCI/PnP devices to use this interrupt
	[Reserved]	Disable using this interrupt by external PCI/PnP devices, reserve it for Legacy devices. Interrupts 3, 4 and 7, 9, 10, 11 are reserved for COM1COM4 and COM5,6, CAN1,2. If these ports are not used, the corresponding interrupts can be allowed for external devices.
DMA Channel 0 DMA Channel 1 DMA Channel 3 DMA Channel 5 DMA Channel 6 DMA Channel 7	DMA channel reservation for internal Legacy devices of Vortex86DX SoC	
	[Available]	Enabling this DMA channel to be used by external PCI/PnP devices
	[Reserved]	Disable using this DMA channel by external PCI/PnP devices; reserve it for Legacy devices.
Reserved Memory Size	BIOS memory reservations for devices on ISA bus	
	[Disabled]	Disable memory reservations by BIOS for ISA devices on the ISA bus. Recommended value.
	[16k], [32k], [64k]	Reserve specified amount of memory for ISA bus devices

5.4 Boot

This tab contains items responsible for the module's boot modes, as well as for selecting the IDE device from which the operating system will be booted. The screen view of the “Boot” menu is shown in Figure 5.11, description of the menu items is given in Table 5.10.

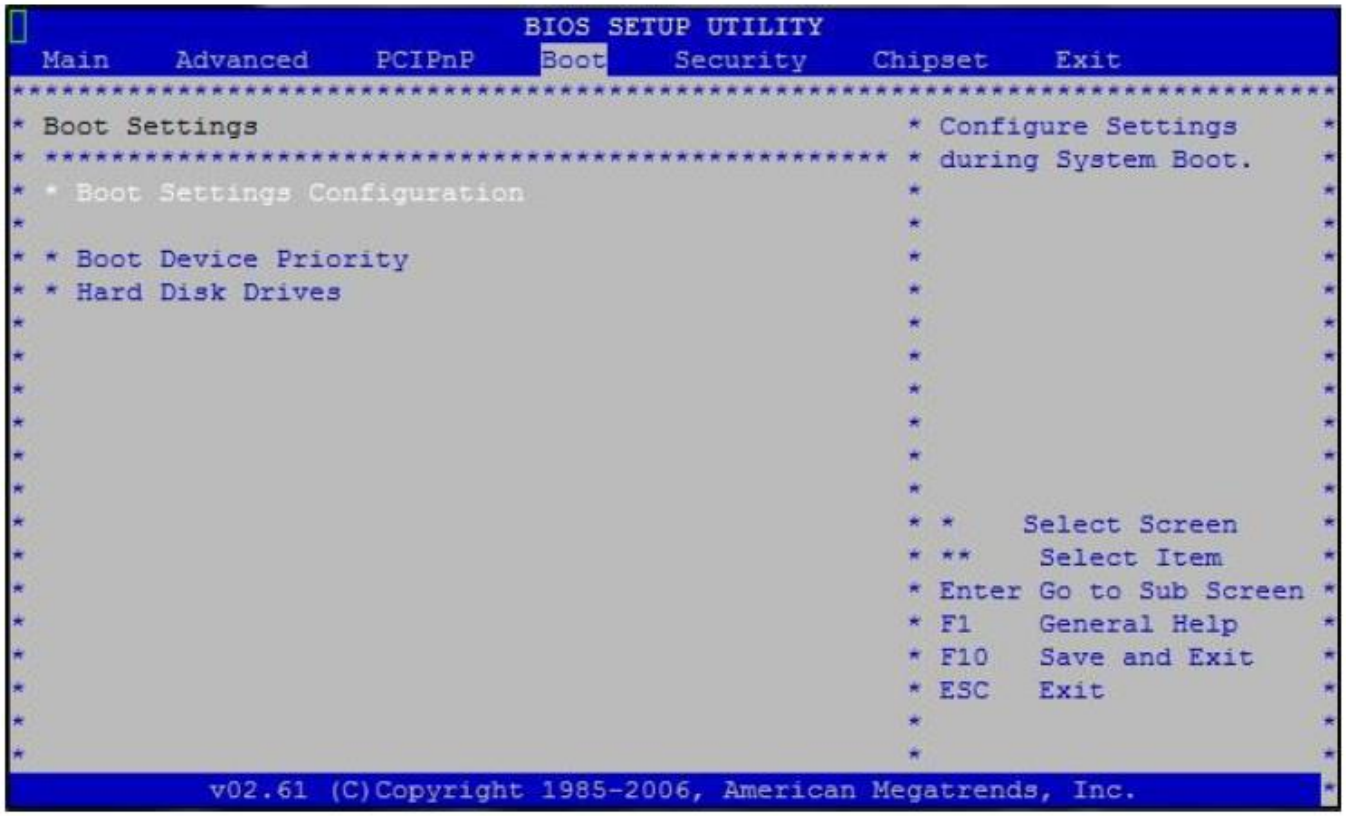


Figure 5.11. Screen of the “Boot” menu

Table 5.10. Description of the “Boot” menu

Menu item	Purpose
Boot Settings Configuration (submenu)	Boot settings Configuration
Boot Device Priority	Priority of selecting the IDE, USB boot devices. When you connect a USB device for the first time or change the configuration of the drives, the booting will be done from USB.
	1st Boot Device – default booting from the selected device
	2nd Boot Device – booting from the selected device will be performed if the 1st Boot Device is not a bootable device.
Hard Disk Drives	The order in which you select the bootable hard disks.
	1st Drive – default boot from the selected hard drive
	2nd Drive – the selected device will be used for booting if the 1st Drive is not a bootable drive

5.4.1 Boot Settings Configuration

The "Boot Settings Configuration" menu screen is shown in Figure 5.12, the description of the menu items is given in Table 5.11.

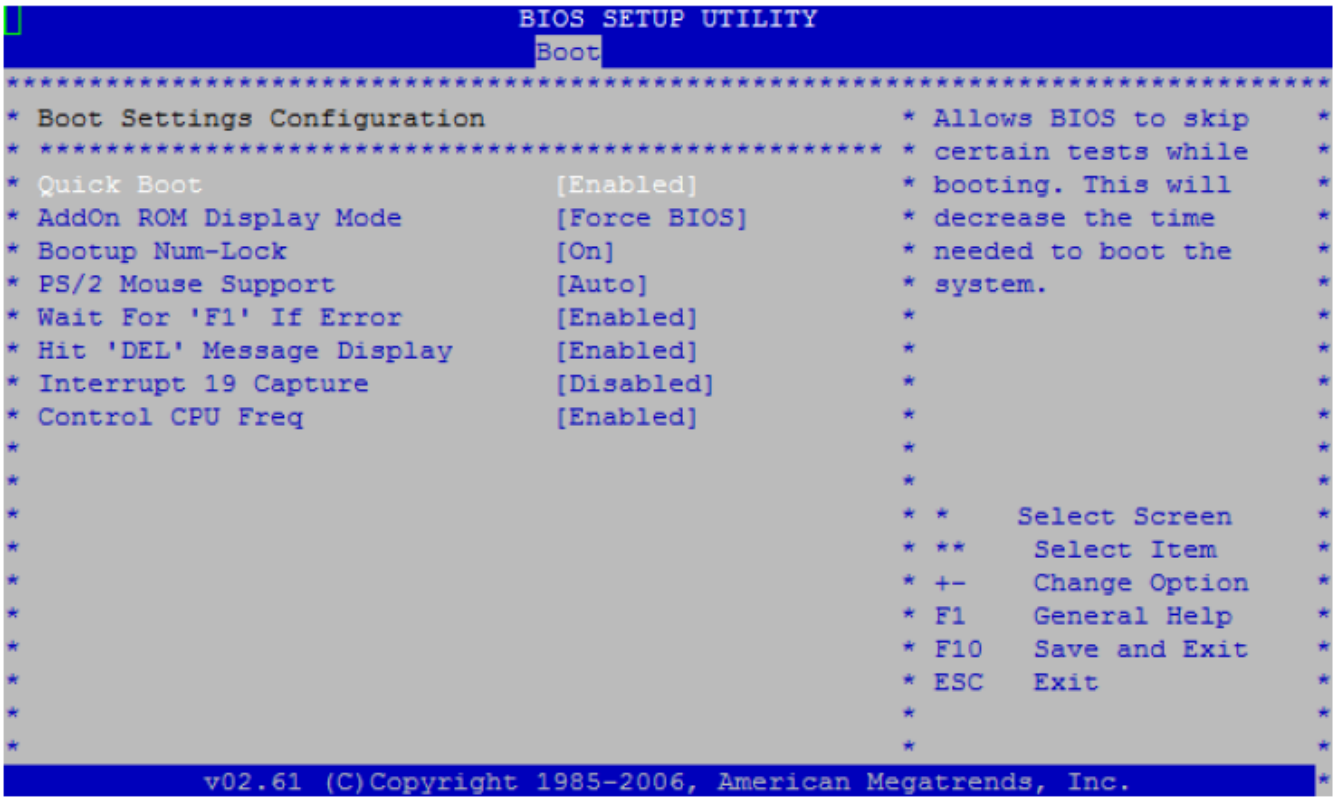


Figure 5.12. Screen of the "Boot Settings Configuration" menu

Table 5.11. Description of the "Boot Settings Configuration" menu

Menu item	Purpose	
Quick Boot	Quick booting	
	[Disabled]	Selecting this value provides a complete the system self-test when switching on
	[Enabled]	Selecting this value reduces the number of tests at power up and thus speeds up the boot process
Add On ROM Display Mode	Expansion card display mode	
	[Force BIOS]	This value enables the monitor to display data from the BIOS expansion cards during system boot
	[Keep Current]	This setting enables the computer system to display only P.O.S.T. information during booting process
Bootup Num-Lock	Numbers lock at boot-up (Num Lock)	
	[Off]	Disabling numbers lock at boot-up
	[On]	Enabling numbers lock at boot-up
PS/2 Mouse Support	PS/2 mouse support	

	[Disabled]	Support is disabled
	[Enabled]	Support is enabled
	[Auto]	Support is detected automatically. Recommended value
Wait for ‘F1’ If Error	Waiting for “F1” key to be pressed in case of error	
	[Disabled]	This option does not require to wait for user intervention in case of an error. You should only choose this option if you know of a reason why a BIOS error might occur.
	[Enabled]	Enabling the BIOS to wait for the user to press the “F1” key if a boot error occurs.
Hit ‘DEL’ Message Display	Display the message “Hit Del to enter Setup” during memory initialization	
	[Disabled]	Message display is disabled
	[Enabled]	Message display is enabled
Interrupt 19 Capture	Capturing INT19 software interrupts	
	[Disabled]	BIOS disables additional controllers to capture INT19 interrupts
	[Enabled]	BIOS enables additional controllers to capture INT19 interrupts
Control CPU Freq	CPU frequency control	
	[Disabled]	Control is disabled
	[Enabled]	Control is enabled

5.5 Security

The “Security” menu screen is shown in Figure 5.13. The description of the menu items is given in Table 5.12.

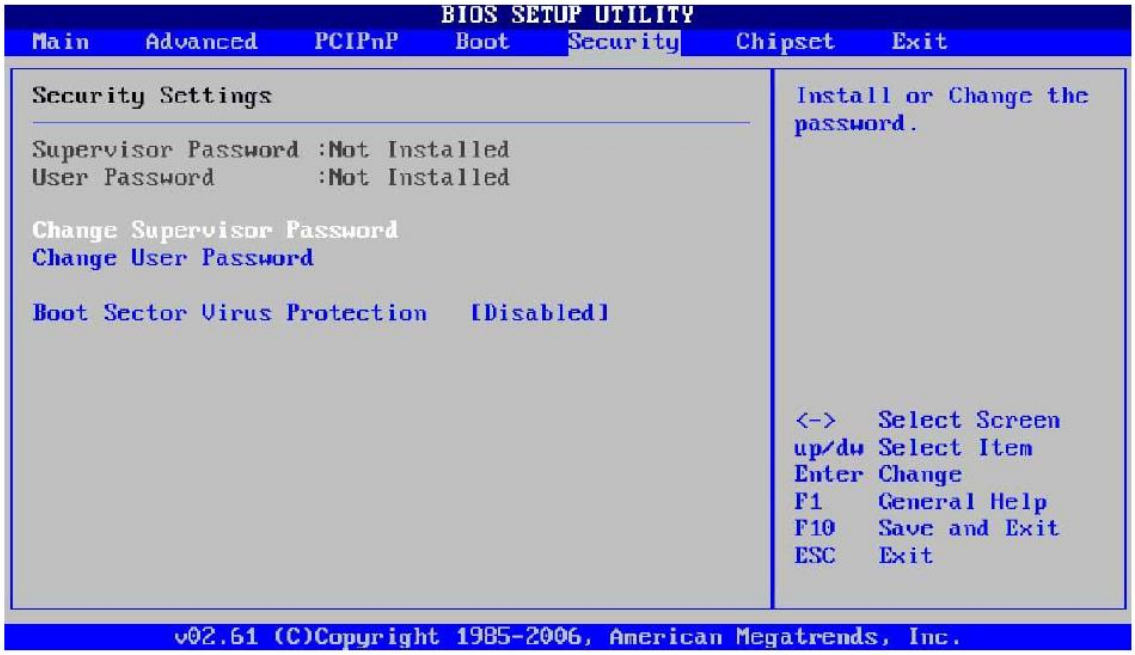


Figure 5.13. Screen of the “Security” menu

Table 5.12. Description of the “Security” menu

Menu item	Purpose	
Change Supervisor Password	Changing the system boot permission password (prompted for during P.O.S.T.)	
Change User Password	Changing the BIOS Setup access password (prompted for while entering BIOS Setup)	
Boot Sector Virus Protection	Boot sector virus protection	
	[Disabled]	Selecting this item will disable protection of the boot sector from viruses.
	[Enabled]	Selecting “Enabled” will enable virus protection for the boot sector. If any program (or virus) performs a disk format command (Disk Format) or tries to write to the boot sector on the hard disk, the relevant warning is displayed on the monitor. If an attempt is made to write to the boot sector while the protection is on, the following messages will appear: Boot Sector Write! Possible VIRUS: Continue (Y/N)?_ You may have to press N several times to prevent writing to the boot sector. The following message appears after any attempt to format any hard drive via BIOS INT 13 Hard disk drive service: Format!!! Possible VIRUS: Continue (Y/N)?_

5.6 Chipset

The “Chipset” menu screen is shown in Figure 5.14. Description of the menu items is given in Table 5.13.

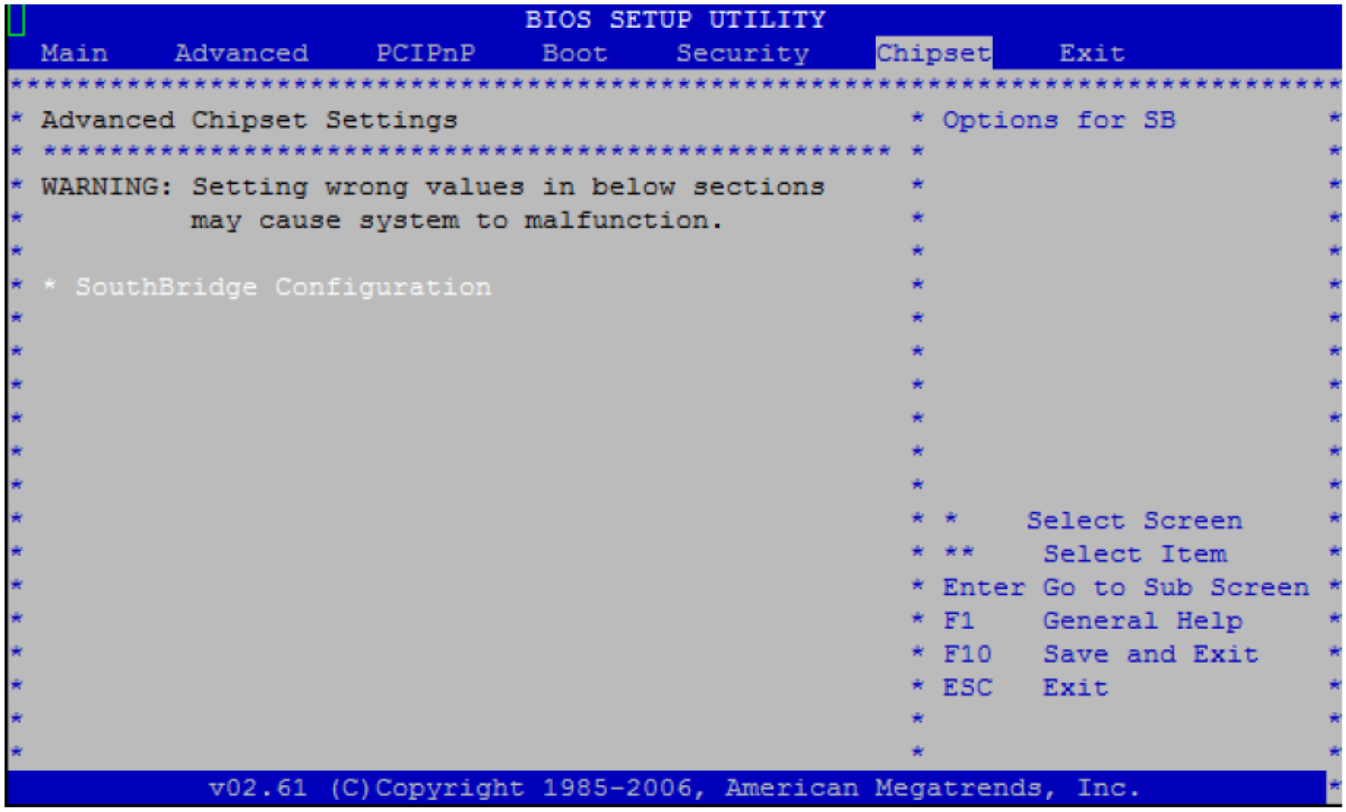


Figure 5.14. Screen of the “Chipset” menu

Table 5.13. Description of the “Chipset” menu

Menu item	Purpose
SouthBridge Configuration (submenu)	SouthBridge Configuration

5.6.1 South Bridge Configuration

The South Bridge Configuration menu screen is shown in Figure 5.15, description of the menu items is given in Table 5.14.

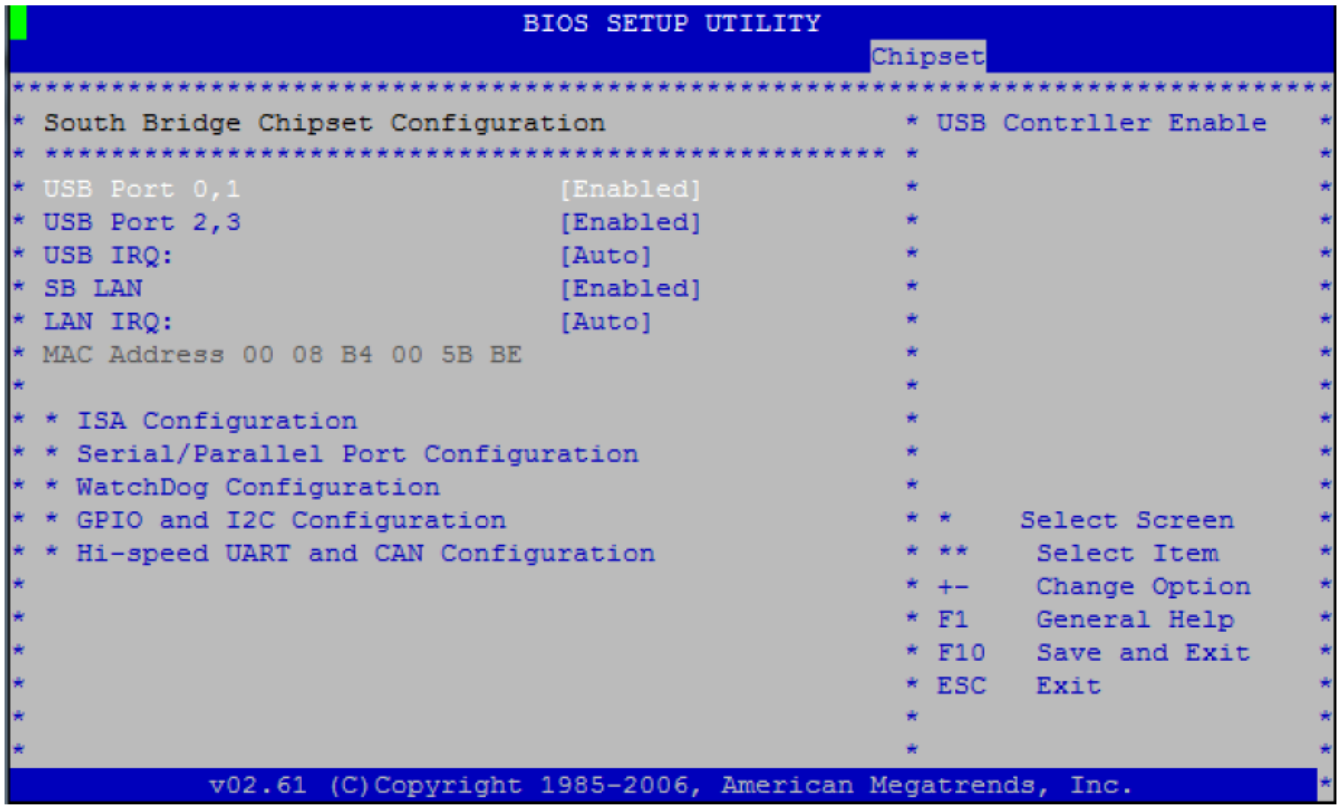


Figure 5.15. Screen of the "South Bridge" menu

Table 5.14. Description of the "South Bridge Configuration" menu

Menu item	Purpose	
USB Port 0,1	Control the operation of USB ports 0 and 1	
	[Enabled]	Enable operation of ports
	[Disabled]	Disable operation of ports
USB Port 2,3	Control the operation of USB ports 2 and 3	
	[Enabled]	Enable operation of ports
	[Disabled]	Disable operation of ports
USB IRQ	Assigning interrupts to USB controller	
	[Auto]	Automatic detection
	[use IRQ 5]	Assign interrupt #5
	[use IRQ 6]	Assign interrupt #6
SB LAN	Controls the operation of the integrated Ethernet (LAN) controller, the MAC address is listed below	
	[Enabled]	Enable controller operation
	[Disabled]	Disable controller operation

LAN IRQ	Assigning interrupt to the Ethernet (LAN) controller	
	[Auto]	Automatic detection
	[IRQ 5]	Assign interrupt #5
	[IRQ 10]	Assign interrupt #10
	[IRQ 15]	Assign interrupt #15
	[IRQ 6]	Assign interrupt #6
MAC Address	MAC address of the integrated Ethernet (LAN) controller	
ISA Configuration (submenu)	This option allows you to set the ISA bus timings for I/O and memory accesses	
Serial/Parallel Port Configuration (submenu)	This option sets the address/mode/interrupt for serial and parallel ports	
WatchDog Configuration (submenu)	Control of the integrated watchdog timers WDT0, WDT1	
GPIO and I2C Configuration (submenu)	Configuration of I/O port GPIO[0]	
CAN and COM5,6 Configuration (submenu)	Configuration of CAN1,2 and COM5,6 ports	

5.6.1.1 ISA Configuration

The “ISA Configuration” menu screen is shown in Figure 5.16, description of the menu items is given in Table 5.15.

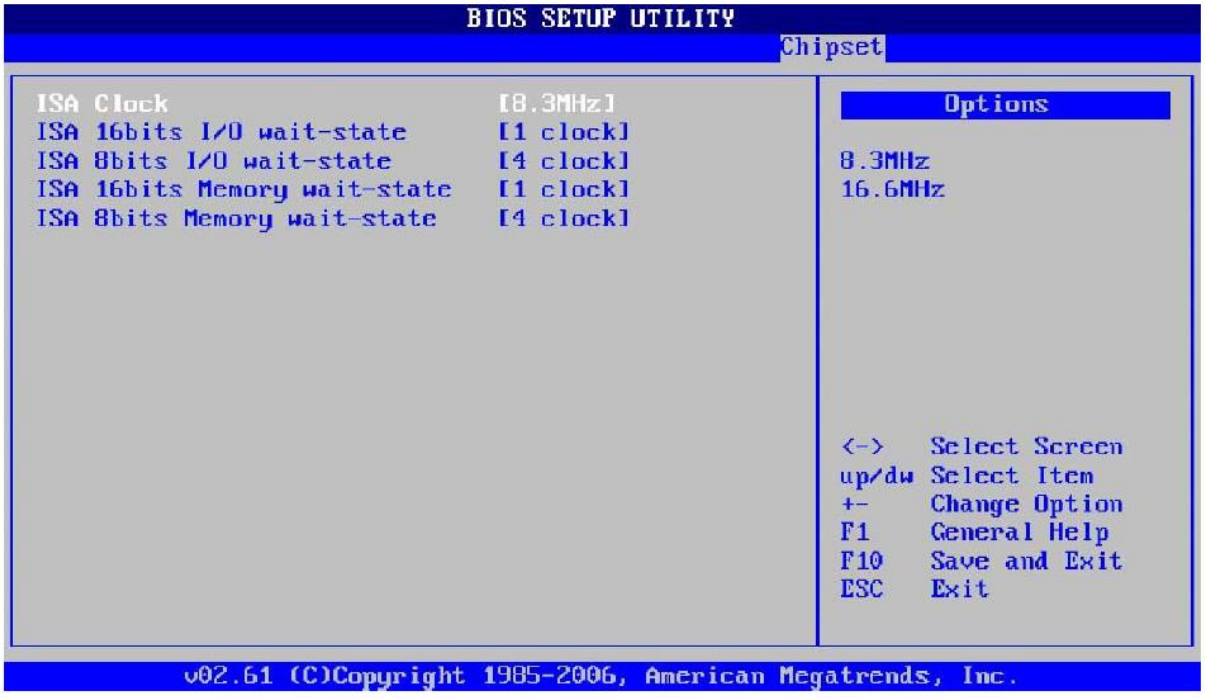


Figure 5.16. Screen of the “ISA Configuration” menu

Table 5.15. Description of the “ISA Configuration” menu

Menu item	Purpose	
ISA Clock	Clock frequency ISA_SYSCLK (CLK, XS2 connector, output B20)	
	[8.3MHz]	Set the clock frequency for 8 MHz
	[16.6MHz]	Set the clock frequency for 16 MHz
ISA 16bits I/O wait-state	I/O wait-state cycle duration at 16-bit reference on ISA bus	
	[1 clock], [2 clock], [3 clock], [4 clock], [5 clock], [6 clock], [7 clock], [8 clock]	
ISA 8bits I/O wait-state	I/O wait-state cycle duration at 8-bit reference on ISA bus	
	[1 clock], [2 clock], [3 clock], [4 clock], [5 clock], [6 clock], [7 clock], [8 clock]	
ISA 16bits Memory waitstate	Memory wait-state cycle duration at 16-bit reference on ISA bus	
	[0 clock], [1 clock], [2 clock], [3 clock], [4 clock], [5 clock], [6 clock], [7 clock]	
ISA 8bits Memory waitstate	Memory wait-state cycle duration at 8-bit reference on ISA bus	
	[1 clock], [2 clock], [3 clock], [4 clock], [5 clock], [6 clock], [7 clock], [8 clock]	

5.6.1.2 Serial/Parallel Port Configuration

The “Serial/Parallel Port Configuration” menu is shown in Figure 5.17, description of the menu items is given in Table 5.16.

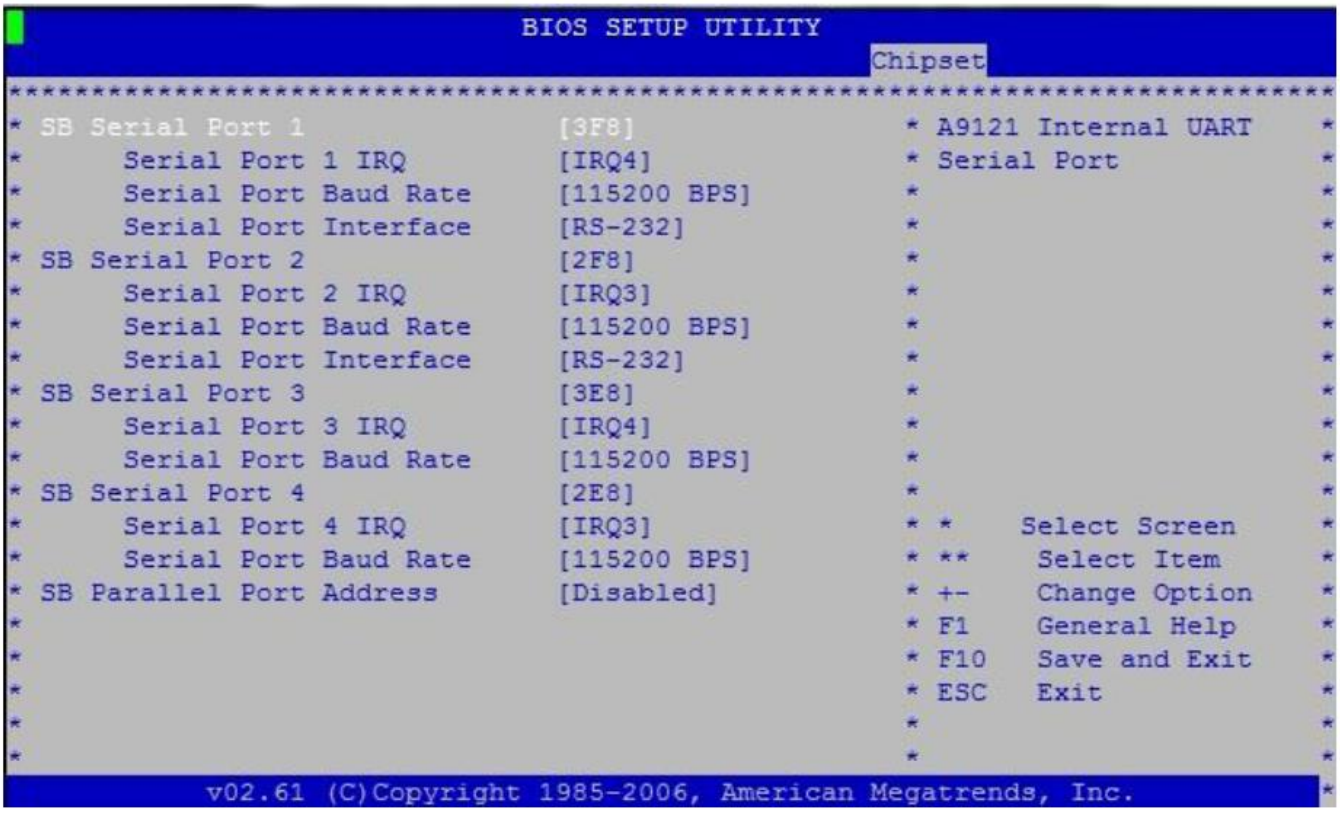


Figure 5.17. Screen of the “Serial/Parallel Port Configuration” menu

Table 5.16. Description of the "Serial/Parallel Port Configuration" menu

Menu item	Purpose	
SB Serial Port 1 SB Serial Port 2 SB Serial Port 3 SB Serial Port 4	This option sets the address for the corresponding serial port (separately for each port)	
	[Disabled]	Port operation is disabled
	[3E8]	I/O Base Address Assignment 3E8h
	[2E8]	I/O Base Address Assignment 2E8h
	[3F8]	I/O Base Address Assignment 3F8h
	[2F8]	I/O Base Address Assignment 2F8h
	[10]	I/O Base Address Assignment 10h
Serial Port IRQ 1 Serial Port IRQ 2 Serial Port IRQ 3 Serial Port IRQ 4	This option assigns an interrupt line for the corresponding serial port (separately for each port)	
	[IRQ3]	IRQ3 Interrupt Line Assignment
	[IRQ4]	IRQ4 Interrupt Line Assignment
	[IRQ9]	IRQ9 Interrupt Line Assignment
	[IRQ10]	IRQ10 Interrupt Line Assignment
	[IRQ11]	IRQ11 Interrupt Line Assignment
Serial Port Baud Rate	This option sets the data exchange speed for the corresponding serial port (for each port separately)	
	[2400 BPS], [4800 BPS], [9600 BPS], [19200 BPS], [38400 BPS], [57600 BPS], [115200 BPS]	
SB Parallel Port Address	This option sets the address for LPT1 parallel port	
	[Disabled]	Port operation is disabled
	[378]	I/O Base Address Assignment 378h
	[278]	I/O Base Address Assignment 278h
Parallel Port Mode	This option sets the operating mode for the LPT1 parallel port	
	[BPP]	Bi-directional Parallel Port (BPP) operating mode The transmit/receive mode for the parallel port
	[EPP 1.9 AND SPP]	Operating mode compatible with EPP 1.9 and SPP modes
	[ECP]	Enhanced Capabilities Port (ECP) operation mode ECP uses the DMA protocol to achieve a symmetrical bidirectional data transfer rates of up to 2.5 Mb/sec.
	[ECP AND EPP 1.9]	Operating mode compatible with ECP and EPP 1.9 modes
	[SPP]	Standard Parallel Port (SPP) operation mode
	[EPP 1.7 AND SPP]	Operating mode compatible with EPP 1.7 and SPP modes. Enhanced Parallel Port (EPP) mode of operation uses existing parallel port signals for asymmetrical bidirectional data transfer from the host device

	[ECP AND EPP 1.7]	Operating mode compatible with ECP and EPP 1.7 modes
Parallel Port IRQ	This option assigns an interrupt line for the LPT1 parallel port	
	[IRQ5]	IRQ5 interrupt line assignment
	[IRQ7]	IRQ7 interrupt line assignment

5.6.1.3 WatchDog Configuration

The Watchdog Configuration menu screen is shown in Figure 5.18, description of the menu items is given in Table 5.17.

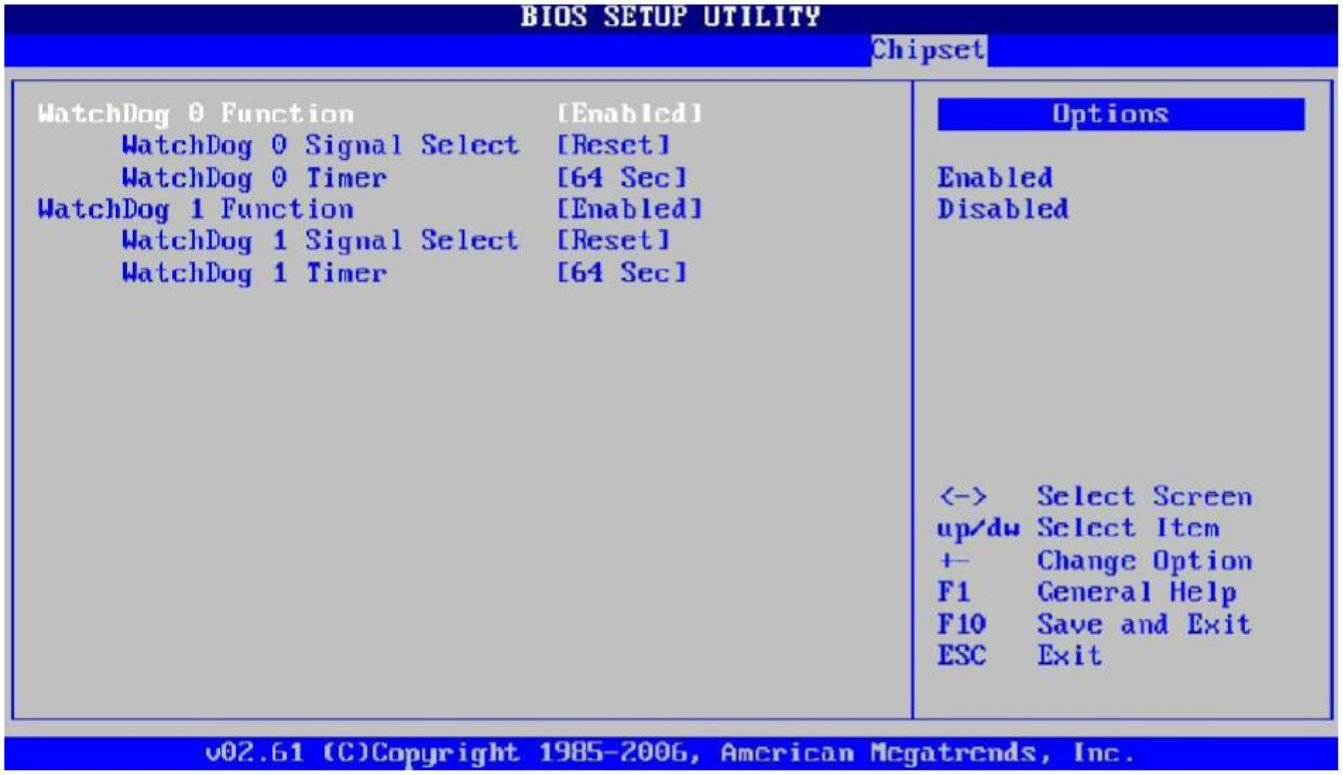


Figure 5.18. Screen of the "WatchDog Configuration" menu

Table 5.17. Description of the "WatchDog Configuration" menu

Menu item	Purpose	
WatchDog 0 Function WatchDog 1 Function	Control of WDT0, WDT1 watchdog timers integrated in Vortex86DX SoC.	
	[Disabled]	Timer operation is disabled
	[Enabled]	Timer operation is enabled
WatchDog 0 Signal Select WatchDog 1 Signal Select	This option allows you to define the action to be selected after the counting time of the corresponding watchdog timer has expired. It is possible to generate one of the interrupts, including a non-maskable interrupt, as well as to generate a reset signal (Reset)	
	[IRQ3], [IRQ4], [IRQ5], [IRQ6], [IRQ7], [IRQ9], [IRQ10], [IRQ11], [IRQ12], [IRQ14], [IRQ15], [NMI], [Reset]	

WatchDog 0 Timer WatchDog 1 Timer	Sets the time interval for the corresponding timer counting. The Watchdog timer counts backwards during operation. If the value is set to 64 seconds, it will count down to 0 and then generate a RESET, NMI or IRQ signal. If the timer receives a reset signal during the countdown, it will interrupt the count and start counting again from 64
	[1 Sec], [2 Sec], [4 Sec], [8 Sec], [16 Sec], [32 Sec], [64 Sec], [128 Sec], [256 Sec], [512 Sec]

5.6.1.4 GPIO and I2C Configuration

Screen of the “GPIO and I2C Configuration” menu is shown in Figure 5.19, description of the menu items is given in Table 5.18.

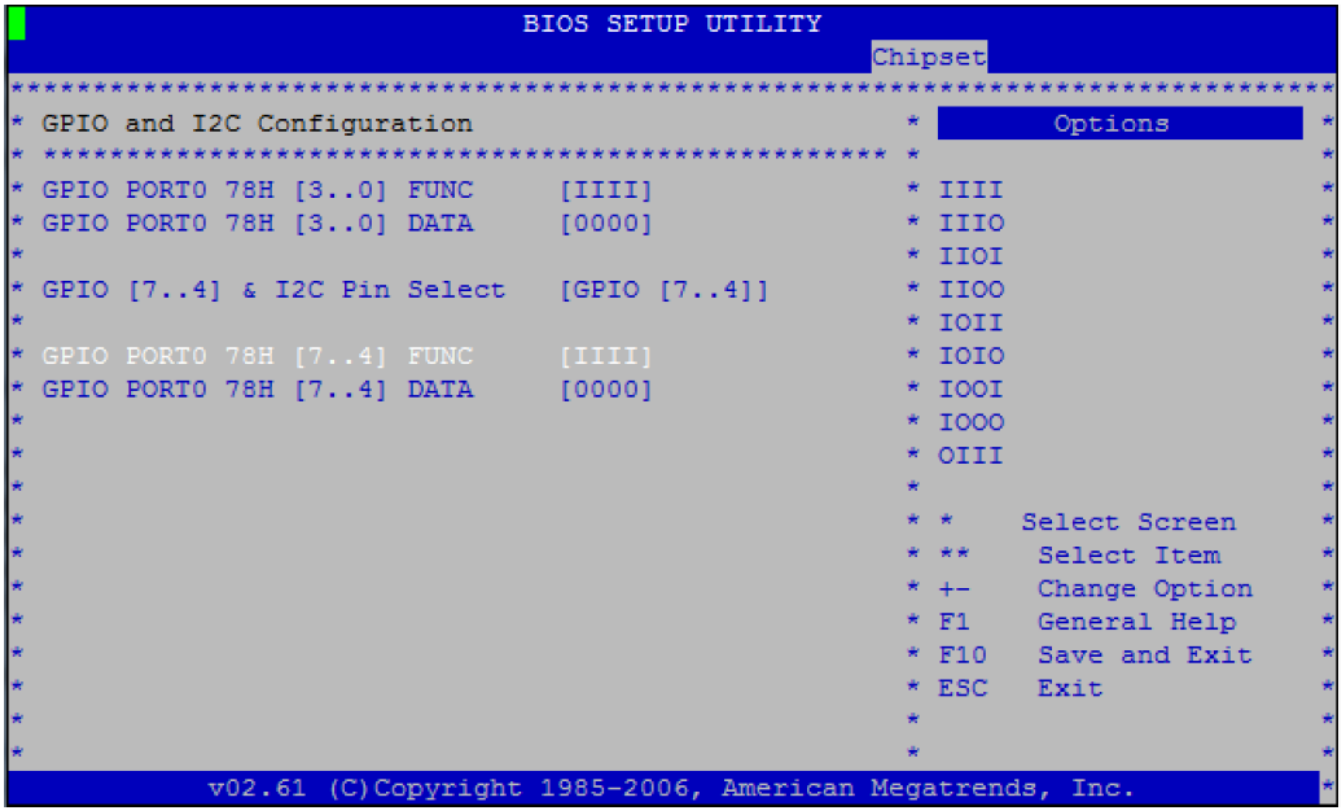


Figure 5.19. Screen of the “GPIO and I2C Configuration” menu

Table 5.18. Description of the “GPIO and I2C Configuration” menu

Menu item	Purpose	
GPIO PORT0 78H [3..0] FUNC	Sets the port lines to “input” or “output” status. Each line can be individually set as “input” or “output”.	
	[*I*]	Line is set as “input”
	[*0*]	Line is set as “output”
GPIO PORT0 78H [3..0] DATA	Sets the output lines of the port to log.1 or log.0 status. Each line can be set to log.1 or log.0 regardless of the status of the other lines	
	[*1*]	Line is set to log.1 (+3.3V) state
	[*0*]	Line is set to log.0 state
GPIO PORT0 78H [7..4] & I2C	Selecting the operating mode of lines [7...4] of GPIO port 0	

Pin Select	[2xI2C Bus]	Two I2C ports
	[GPIO [7..4]]	Lines of the GPIO 0 I/O port
GPIO PORT0 78H [7..4] FUNC	Sets the port lines to “input” or “output” state. Each line can be individually set as “input” or "output	
	[*I*]	Line is set as “input”
	[*0*]	Line is set as “output”
GPIO PORT0 78H [7..4] DATA	Sets the output lines of the port to log.1 or log.0 status. Each line can be set to log.1 or log.0 regardless of the status of the other lines	
	[*1*]	Line is set to log.1 (+3.3V) state
	[*0*]	Line is set to log.0 state

5.6.1.5 CAN and COM5,6 Configuration

The screen of the “CAN and COM5,6 Configuration” menu is shown in Figure 5.20, description of the menu items is shown in Table 5.19.

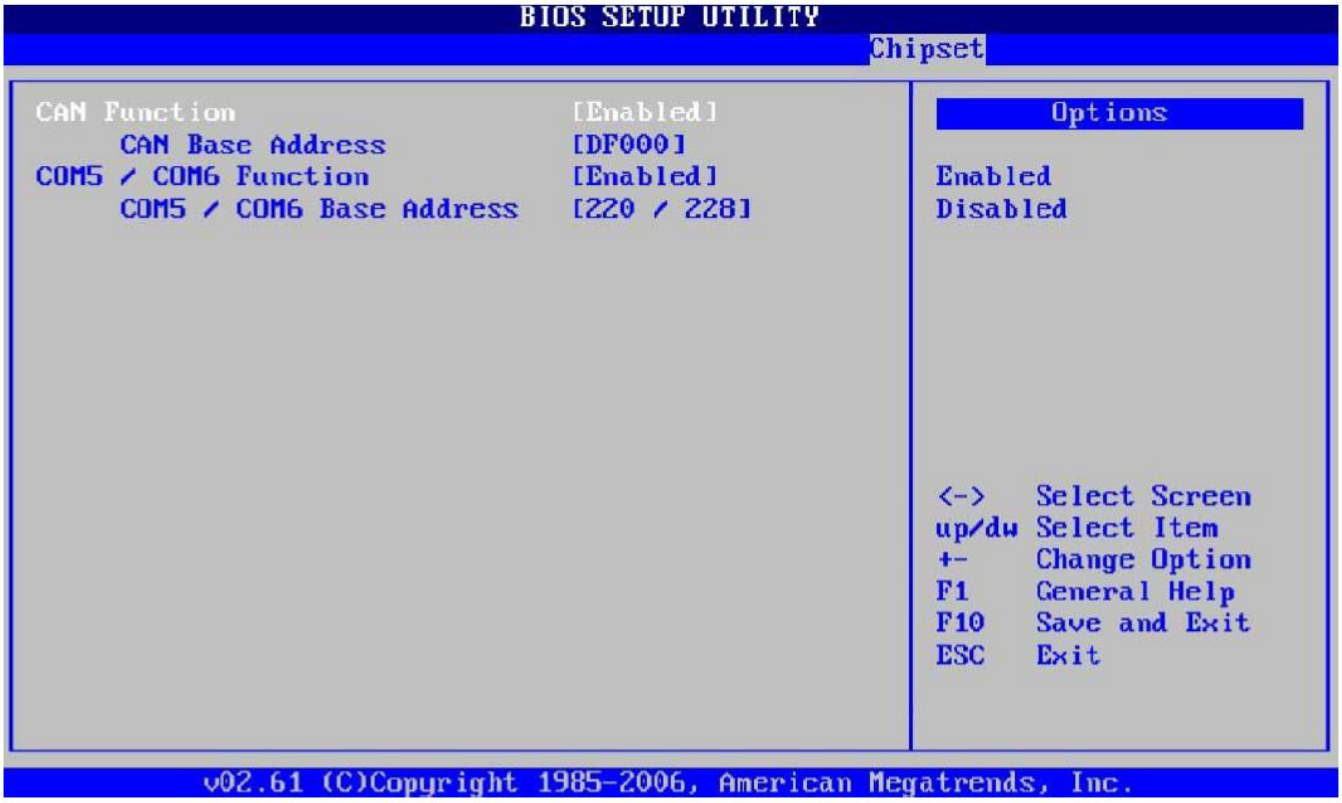


Figure 5.20. Screen of the “CAN and COM5,6 Configuration” menu

Table 5.19. Description of the “CAN and COM5,6 Configuration” menu

Menu item	Purpose	
CAN Function	Control of CAN1, CAN2 ports operation	
	[Enabled]	Address decoding is enabled, ports are available for programming
	[Disabled]	Address decoding is disabled, ports not available for programming
CAN Base Address	Specifying base address for CAN1, CAN2 ports. 4 base addresses are available: [CE000], [CF000], [DE000], [DF000]	
COM5 / COM6 Function	Control of COM5, COM6 operation	
	[Enabled]	Address decoding is enabled, ports are available for programming
	[Disabled]	Address decoding is disabled, ports not available for programming
COM5 / COM6 Base Address	Specifying base address for COM5, COM6 ports 4 base addresses are available: [220 / 228], [240 / 248], [320 / 328], [340 / 348]	

5.7 Exit

The “Exit” menu screen is shown in Figure 5.21. Description of the menu items is given in Table 5.20.

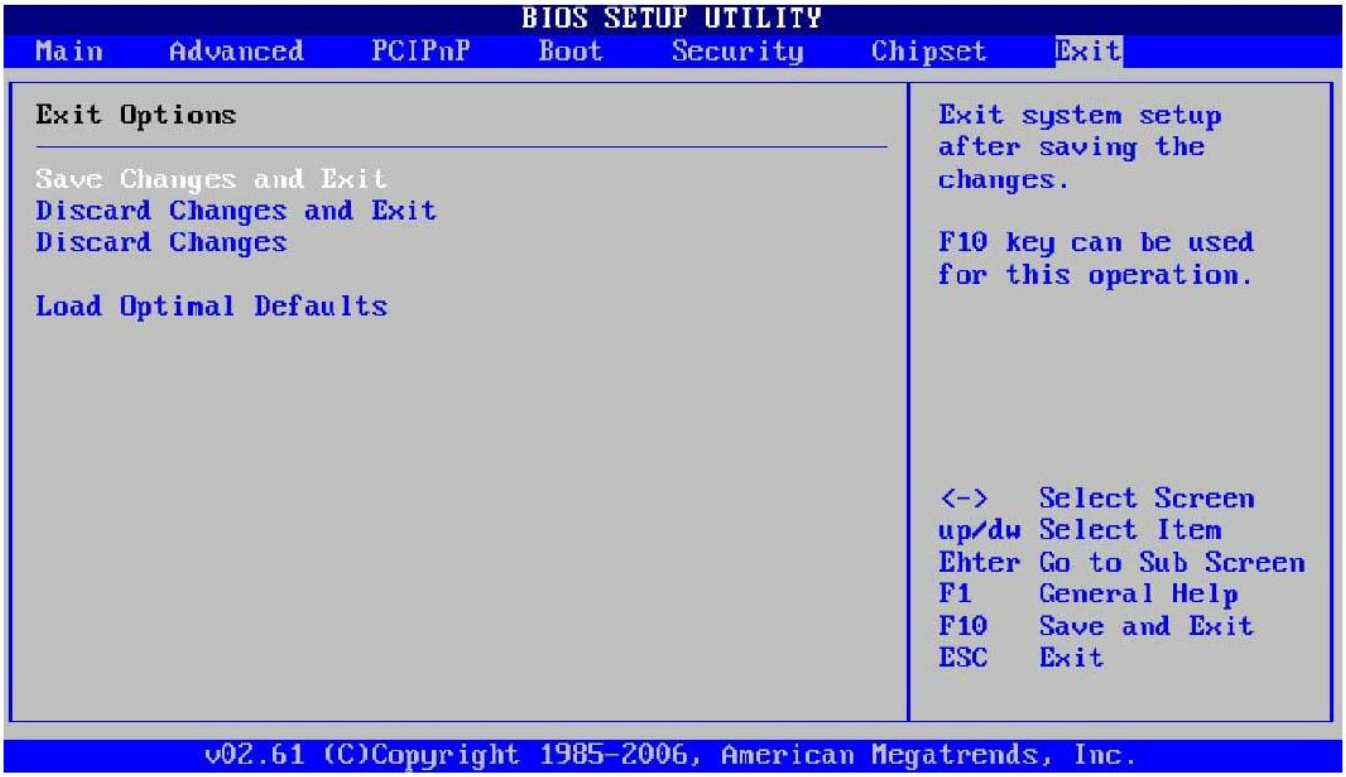


Figure 5.21. Screen of the “Exit” menu

Table 5.20. Description of the “Exit” menu

Menu item	Purpose
Save Changes and Exit	Save changes in settings of the CMOS and FRAM memory and exit BIOS Setup
Discard Changes and Exit	Exit without saving changes in settings in the CMOS and FRAM memory
Discard Changes	Discard changes made to the settings without exiting BIOS Setup program
Load Optimal Defaults	Load optimal (factory) settings without exiting BIOS Setup

5.8 Functional limitations of BIOS versions

BIOS version 3.12 (Core Version 8.00.15, build date 31/01/2012) pre-installed in modules version 3.1, has the following functionality limitations:

1. Skipping the load of Autoexec.bat by the Ctrl+B command through the input/output console has been adjusted.

2. Console I/O for COM2 port has been adjusted.

3. The IDE port operating mode is limited to UDMA0 mode for the purpose of enhancing stability of the system with various IDE devices under extreme ambient temperatures.

BIOS version 3.11 (Core Version 8.00.15, build date 11/02/2011) pre-installed in modules version 3.1 has the following functionality limitations:

1. Console I/O to port COM2 integrated into BIOS is not working. It is recommended to use COM1, 3, 4 ports for utilizing the integrated console input/output.

BIOS version 2.0 (Core Version 8.00.15, build date 01/20/2010), pre-installed in modules version 3.0, has the following functionality limitations:

1. When operating in “Native Mode” of IDE controller, with the “PCI IDE BusMaster – Enabled” and “ATA(PI) 80Pin Cable Detection – Device” options set, ATA Flash drive malfunctions are possible.

BIOS version 1.1 (Core Version 8.00.14, build date 11/24/2009), pre-installed in modules version 3.0, has the following functionality limitations:

1. No DMA support on the IDE bus (was fixed in BIOS version 2.0).

2. No USB keyboard and mouse support (was fixed in BIOS version 2.0).

3. Module takes a long time to boot if there is only one IDE device (was fixed in BIOS version 2.0).

6 Guidelines on operation and use

The module must be used in the modes and under the conditions described in the User Manual and technical specifications for “Industrial embedded computer in PC104 format” (TS 4013-004-52415667-05).

The module must be supplied with power from an external DC source with fixed voltage value of +5 V ± 5%.

Connecting (disconnecting) external devices and expansion boards to (from) the module when the module is on is prohibited.

Connecting (disconnecting) the module to (from) an external DC source while the module is on is prohibited.

Connecting external devices and expansion boards to the module must be performed in accordance with the User Manual.

It is not allowed to connect external equipment and communication interface cables without disconnecting the module’s power supply and the connected external equipment.

Before installing the board in the system, make sure that the mains power supply is disconnected. The same also applies to the installation of expansion boards. Electronic boards and their components are sensitive to static electricity. Therefore special care and particular attention are required when handling these devices to ensure their safety and proper performance.

Attention!

The PC104 and PC104+ expansion module with PCI connector can be installed in one PC104 stack with a CPC307 module:

• if there is no PCI connector organizer on the expansion module: neither on the top, nor on the bottom side of the CPC307 module;

• where there is a PCI connector organizer on the Expansion Module: installation would be possible only on the bottom side of the CPC307 module.

7 Existing limitations and special features of the CPC307 module (ERRATA)

In the CPC307, PP 687263.012 v3.x modules, disabling the internal storage (NAND Flash) during operation is impossible.

Annex A
List of changes in the module version 4.x

1. Switching of bias resistors for RS-422/485 ports has been changed.

2. Integrated drive capacity has been increased to 2 GB.

3. Additional XP27 jumper for reset of BIOS settings has been implemented BIOS.

4. Protection against polarity reversal, short-circuit while supplying power through additional power connector XP22 has been implemented.

5. Soft start is arranged to reduce starting current. Active overvoltage protection up to 30V is implemented when power is supplied via additional power connector.

6. Switching diagram of matching resistors of CAN ports has been changed.

7. In versions older than 4.x, the WDT2 watchdog can be switched off by setting the jumper to the XP26 connector. In module versions 4.x, the opposite is true: placing a jumper on the XP26 enables the WDT2 watchdog, while removing the jumper disables it.

8. There are two copies of BIOS stored in the module (for versions older than 4.x) - main and backup. When you turn on the power supply the module always boots from the main BIOS copy. If the external watchdog in the ADM706T power supply supervisor chip is activated the module will restart. There is no backup copy of the BIOS for the 4.x versions of the module.

9. In version 4.x the BIOS updating procedure has been changed.

10. In version 4.x, if the XP24[2-3] jumper is installed, the onboard drive is disabled. There was no such feature in 3.x versions.

11. The DDR2 RAM frequency has been increased to 333 MHz (was 266 MHz).

ANNEX:B DISCLAIMER

This Disclaimer contains special operating conditions of Fastwel in the following areas: intellectual property, warranty policy, conditions of the order and delivery.

1 INTELLECTUAL PRORETY

1.1 If any infraction, interference, improper use, illegitimate exploitation and/or violation of the industrial and/or intellectual property rights of any third party and/or property, exploitation during the use of Fastwel Embedded Module will take place – Fastwel does not guarantee to replace the materials, computer programs, procedures or equipment affected by the complaint and under no circumstances doesn't bear responsibility in any form for possible refusal in case of such a replacement.
1.2 Use of the Fastwel products as well as the objects of intellectual property containing in them, in the ways and for the purposes, not provided by the present user manual and datasheet isn't allowed without preliminary written approval of Fastwel.
1.3 Fastwel is not responsible for possible incidents and losses, related to the operation of end devices, in which the original Fastwel equipment is used.

2 WARRANTY POLICY

2.1 When the detected flaws in an element can be corrected without decreasing the foreseen technical features and functionality for it, User may demand Fastwel the urgent correction of the failures in additionally agreed period and an increasing of the period of the guarantee of the element equal as the time elapsed from the formal request to repair the failures, until the receipt of the repaired element. All costs associated to the correction of failures, included those of assembly, dismantle, transport, tests, etc, if they exist, shall be prosecuted according the Warranty Policy of Fastwel.

3 ORDER AND DELIVERY CONDITIONS

3.1 The general rule is that all Fastwel equipment prices are determined with due consideration of delivery under the EXW terms and conditions (Incoterms 2010). Delivery of the products under other terms and conditions should be preliminary agreed and stated in writing between the parties.
3.2 Unless otherwise expressly agreed with Fastwel, all the deliveries of Fastwel equipment will be carried out only after the official purchase order is obtained and provided that the ordered products have been prepaid in full. Other terms and conditions of cooperation should be made in writing.
3.3 Any delivery of Fastwel electronics is submitted with the right package in accordance with the current rules and standards in the Member States of the European Economic Area. The purchaser independently bears all risks regarding the compliance of package and marking of Fastwel products with legislation requirements being in effect at the place of purchased products destination (in the buyer's country). The specified condition excludes unequivocally any liability of Fastwel for possible non-compliance of package and marking of products with the requirements of legislation of the country of products destination.
3.4 In general, all components of the supply are properly protected with respect to freight, in order to avoid any damage to the supply, third parties, environmental damages or unrelated goods, as consequence of wrong packaging.
3.5 Each package unit is labeled on the exterior area with the indications of product's Part Number and Serial Number.
3.6 The support documents for the order should be made either in English or in Russian unless otherwise agreed between parties in writing.
3.7 Fastwel does not pay penalties and does not cover costs associated with delay in the delivery of the products caused by actions of the third parties, force-majeure etc. - Fastwel doesn't bear any responsibility for non-execution or inadequate execution of the obligations in a case when it is caused by actions of the third parties (for example producers or suppliers of accessories), force majeure etc.
3.8 Fastwel declares that independently and at any time without damage, it has an exclusive right to define and change functionality architecture, bill of materials of its products without any preliminary coordination and approvals of the third parties.

4 OTHER CONDITIONS

4.1 Fastwel has the obligation to respect the current Russian legislation (including, but not limited to environmental, labor, social laws) in each moment and to apply it to its embedded electronics considering all and each execution phase, that is to say, from the design until the commissioning and subsequent maintenance. In this regard Fastwel is not liable to the user or other persons in connection with possible changes of the company's rules (including, but not limited to warranty, ordering policy) caused by changes of the Russian legislation.
4.2 Unless otherwise expressly agreed in writing, Fastwel provides no training for assembly\installation\adjustment\operation of its equipment.