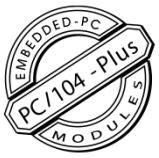


# AIC324

**Analog and Digital Input / Output Module**

# User Manual

July 2018

Version 1.7.1

Product Title: AIC324
Document name: AIC324 User Manual
Manual version: 1.7.1


## Revision Record

| Revision number | Brief description of changes | Device name | Revision date |
|---|---|---|---|
| 1.0 | Initial version | AIC324 | October 2011 |
| 1.1 | Remarks related to the archives | AIC324 | November 2012 |
| 1.2. | Section 1.2.3. has been updated | AIC324 | November 2012 |
| 1.3. | Section 2.1.5. has been added | AIC324 | February 2013 |
| 1.4. | Section 1.1.5 has been added, Annex B 2 has been updated. | AIC324 | April 2013 |
| 1.5. | Labeling has been revised. Weight has been specified. | AIC324 | April 2013 |
| 1.6. | Weight of the device and weight of shipping containers has been added. | AIC324 | June 2013 |
| 1.7. | Section 1.1.5 has been revised. | AIC324 | March 2014 |
| 1.7.1. | Compliance assessment. | AIC324 | July 2018 |

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## Trademarks

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## Ownership Rights

# Notation and Conventions

**Warning!**
**ESD Sensitive Device!**

This symbol draws your attention to the information related to electro static sensitivity of your product and its components. To keep product safety and operability it is necessary to handle it with care and follow the ESD safety directions.

**Warning!**

Information marked by this symbol is essential for human and equipment safety.
Read this information attentively, be watchful.

**Note**

This symbol and title marks important information to be read attentively for your own benefit.

This User Manual (hereinafter referred to as the User Manual) is designed for getting acquainted with the device, its principle of operation and main information, required for the commissioning, intended use and servicing of the device “Analog and Discrete Input / Output Module AIC324” (hereinafter referred to as the Module).

**Note**

The list of the approved abbreviations and notations, used in this User Manual, is specified in Annex A.

Information on the types of hazardous exposure, general requirements and electrostatic safety requirements when preparing the module for use are specified in p.2.1.1 – 2.1.3 of this User Manual.

**WARINING: THE MODULE CONTAINS ESD COMPONENTS!**

# MANUFACTURER'S WARRANTIES

## Warranty liabilities

The manufacturer hereby guarantees that the device meets the technical specification requirements.
The Consumer should comply with the conditions of usage, transportation, storage, installation and assembly, set by the accompanying documents.

The Manufacturer hereby guarantees that the products supplied thereby are free from defects in workmanship and materials, provided operation and maintenance norms were observed during the currently established warranty period. The Manufacturer's obligation under this warranty is to repair or replace free of charge any defective electronic component being a part of a returned product.

Products that broke down through the Manufacturer's fault during the warranty period will be repaired free of charge. Otherwise the Consumer will be invoiced as per the current labor remuneration rates and expendable materials cost.

## Liability limitation right

The Manufacturer shall not be liable for the damage inflicted to the Consumer's property because of the product breakdown in the process of its utilization.

## Warranty period

The warranty period for the products made by Fastwel LLC is 36 months since the sale date (unless otherwise provided by the supply contract).

The warranty period for the custom-made products is 60 months since the sale date (unless otherwise provided by the supply contract.

## Limitation of warranty obligations

The above warranty obligations shall not be applied:

- To the products (including software), which were repaired or were amended by the employees, that do not represent the manufacturer. Exceptions are the cases where the customer has made repairs or made amendments to the devices in the strict compliance with instructions, preliminary agreed and approved by the manufacturer in writing;
- To the products, broken down due to unacceptable polarity reversal (to the opposite sign) of the power supply, improper operation, transportation, storage, installation, mounting or accident.

## Procedure of device returning for repairs

Sequence of activities when returning the products for repairs:

- Apply to Fastwel company or to any of the Fastwel's official representatives for the Product Return Authorization;
- Attach a failure inspection report with a product to be returned in the form, accepted by the Manufacturer, with a description of the failure circumstances and symptoms;
- Carefully package the product in the antistatic bag and carton box, in which the product had been supplied. Then package the product in a safe container for shipping. Failure to package in antistatic material will VOID all warranties.
- The customer pays for shipping the product to Fastwel or to an official Fastwel representative or dealer.

# 1 GENERAL INFORMATION

## 1.1 PURPOSE AND TECHNICAL CHARACTERISTICS OF THE MODULE

### 1.1.1 Purpose of the module

The analog-to-digital input/output module is designed for input and output of analog and digital signals from real-time control systems, production control, high-speed data collection and processing. In addition, the module enables prompt replacement of the working software of the built-in FPGA, which provides additional opportunities for adapting the module to specific tasks.
The module has a partial program compatibility mode with the DMM-32DX-AT card manufactured by Diamond System Corporation. This mode implies the presence of FPGA firmware that repeats the functional load of the DMM-32DX board.

**Module technical features**

The module is made in the PC104 standard and has the following I/O channel structure:

32x galvanically isolated analog inputs (XP9 connector, see fig. 1.1);

4x galvanically isolated analog outputs (XP9 connector, see fig 1.1);

30x digital I/Os (XP12 connector, see fig. 1.1)

**Module power supply:**

Power supply voltage –+5 V ±5% is supplied via PC104 system connector;

Consumption – no more than 0,6 A

insulation strength of analog path 1000V

**Operation conditions:**

operating temperature range – from - 40° C to +85° C;

Relative humidity – from 5 to 95 % at +25° C (no condensation);

**Mechanical characteristics:**

vibration resistance, acceleration amplitude – 10 g, within the range of frequencies 5 … 2000 Hz GOST 28203-89 (IEC 60068-2-6);

resistance to single shocks, peak acceleration – 150 g GOST 28213-89 (IEC 60068-2-27);

resistance to multiple shocks, peak acceleration – 50 g GOST 28215-89 (IEC 60068-2-29).

**MTBF:**

- No less than 100 000 hours.

**Electromagnetic compatibility:**

industrial radio interference from Information Technology Equipment – Class A GOST R 51318.22-99 (CISPR 22-97);

resistance to electromagnetic interference – II-nd group GOST R 50839-2000 (BS EN 61000-6-2:2001)

**Dimensions, no more than:**

105.2 x 96.0 x 23,3 mm.

**Weight: no more than:**

0.12 kg.

**Note –** The MTBF values are calculated using the Telcordia Issue 1 calculation model (calculation method Method I Case 3) for continuous operation in case of the ground-based installation under conditions corresponding to the climatic category 4 as per the GOST standard 15150-69, at the ambient temperature of + 30°C.

### 1.1.2 Characteristics of Analog-to-Digital Converter

number of bits: 16 bits;

Maximum conversion frequency: 250 kHz;

32x analog channels, configurable to 32 asymmetrical, 16 differential,8 differential + 16 asymmetrical;

Ranges of input voltages: 0..0,625 V, 0..1,25 V, 0..2,5 V, 0..5 V, 0..10 V, ±0,625 V, ±1,25 V, ±2,5 V, ±5 V, ±10 V;

Possibility of working with current sensors in the range 0..20 mA, 0..10 mA, 0..5 mA;

Conversion time on each analog input, without averaging – no more than 4 μs;

Input impedance of analog input – no less than 1 MΩ;

Bypass resistance for measuring current of analog input port: 249 Ohm ± 0.05%, 5ppm, 0.125W;

Availability of FIFO buffer for 2048 words ADC;

Availability of channel-scanning mode;

Availability of the function of program calibration of the board's analog paths;

Protection of inputs against overvoltage: ±40V;

Availability of galvanic insulation.

### 1.1.3 Characteristics of Digital-to-Analog Converter

Number of bits: 16 bits;

Setup time – no more than 6 μs;

4 analog outputs;

Output voltages range: 0..5 V, 0..10 V, ±2,5 V, ±5 V, ±10 V;

Maximum output current 3 mA;

Protection of outputs against overvoltage ±40V;

Availability of a ring-buffer for 2048 words DAC;

Availability of the function of program calibration of the board's analog paths.

### 1.1.4 Characteristics and possibilities of digital inputs/outputs

24x I/O channels, analog m/s 8255;

Bus integrability;

Output voltage level 5V CMOS;

support of 16x and 32x bit counters;

ESD protection;

### 1.1.5 Maximum measurement deviations and currents and voltages generations

| ADC measurement range | Limits of the maximum basic percentage error, ±, % | |
|---|---|---|
| | Under normal conditions | Within operating temperature range |
| 0..0,625V | 0,1 | 0,1 |
| 0..1,25V | 0,1 | 0,1 |
| 0..2,5V | 0,1 | 0,1 |
| 0..5V | 0,1 | 0,1 |
| 0..10V | 0,1 | 0,1 |
| ±0,625V | 0,1 | 0,1 |
| ±1,25V | 0,1 | 0,1 |
| ±2,5V | 0,1 | 0,1 |
| ±5V | 0,1 | 0,1 |
| ±10V | 0,1 | 0,1 |
| 0 … 20 mA | 0,2 | 0,2 |
| 0 … 10 mA | 0,2 | 0,2 |
| 0 … 5 mA | 0,2 | 0,2 |

| DAC measurement range | Limits of the maximum basic percentage error, ±, % | |
|---|---|---|
| | Under normal conditions | Within operating temperature range |
| 0… 5 V | 0,1 | 0,1 |
| 0 … 10 V | 0,1 | 0,1 |
| -2,5 … +2,5 V | 0,1 | 0,1 |
| -5 … +5 V | 0,1 | 0,1 |
| -10 … +10 V | 0,1 | 0,1 |

**Note:** These characteristics are received during measurement with the averaging over 32 points and in accordance with MI 2539-99.

# 1.2 MODULE'S STRUCTURE AND FUNCTIONING

## 1.2.1 Location of main components

Location of the main components (including connectors for module's external connections) is given in figure 1.1. Reference notations of connectors in figure correspond to the notations on the board.

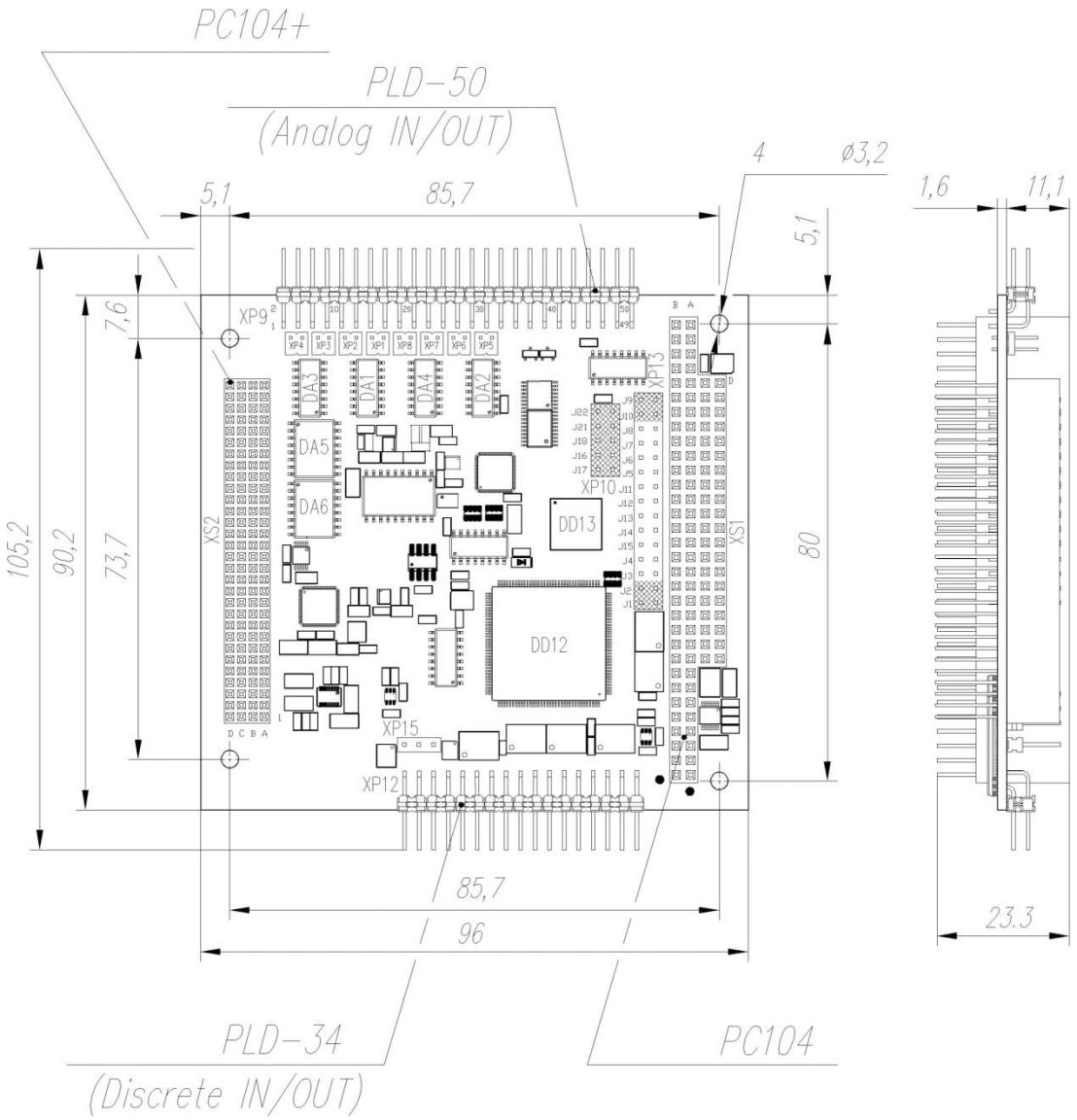



**Figure 1.1 – Main Components and Connectors Layout**

### 1.2.2 Block Diagram

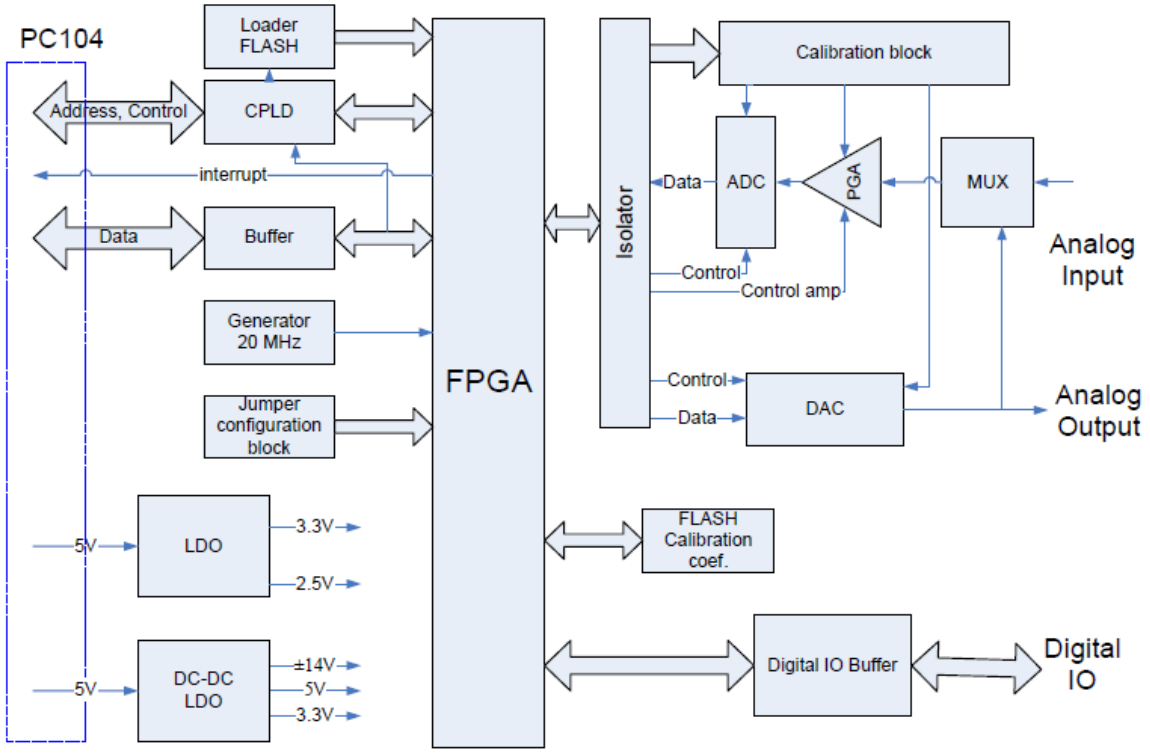



**Figure 1.2 – Module's Block Diagram**

The module includes the following functional blocks:

- Galvanically isolated digital and analog I/O unit.
- Digital I/O unit compatible with 8255.
- Timer unit compatible with 8254.

The analog I/O unit (XP9 connector) consists of a 16-bit ADC with a multiplexed 32x channel input, a 16-bit 4x channel DAC, a path calibration system, a temperature sensor and a digital input/output channel. The multiplexed inputs of the ADC can be configured in 16 differential inputs or 32 non-differential inputs. With the use of jumpers XP1 - XP8 in differential mode, the 0 – 15 differential channels can be transferred to the current measurement mode by connecting current-measuring resistors. The ADC can operate in unipolar and bipolar conversion modes. The path gain factor can be changed from 0.5 to 8 with respect to the reference voltage of 5V. The calibration system makes it possible to perform internal calibration of the board without the use of external means. The calibration minimizes board measurement errors throughout the operating temperature range, and availability of a thermal sensor allows you to save calibrations in nonvolatile memory for reuse when the board is operating in the similar temperature modes. When performing calibration, it is not necessary to disconnect the ADC input channels from the signal sources. When DAC calibration is performed, the output channels must be disconnected, since the DAC generates voltages in the range of ± 10V at the output. Calibration can be performed using the test program aictest ("Aictest program. User Manual") or using functions from the function library supplied with the board ("Functions Library: User Manual"). Digital channels located in the galvanically isolated part of the board, have a fixed direction of input/output and can be used both for the arrangement of synchronous operation of several boards and for implementing digital I/O functions.

The digital I/O unit (XP12 connector) is compatible with an 8255 chip. Port A supports operation in the 0 and 1 modes, the other ports - only in the mode 0. The additional port D consists of 6 I/O lines. All ports have current-limiting protective resistors and the ability to “pull down” or pull up the lines.
The timers unit located on the board is compatible with an Intel 8254 chip and is represented by a three 16-bit timers. Timers 0 and 1 are connected in a circuit, which allows implementing a wide range of frequencies for controlling the operation of ADC and DAC. The control circuits of the timers are output to a galvanically isolated digital I/O port.

### 1.2.3 Module’s distinctive features

Module’s distinctive features are:

- Availability of galvanic isolation of the analog path of the board from the system bus;
- Support of I/O addresses on the PC104 bus: 0x100, 0x140, 0x180, 0x200, 0x280, 0x300, 0x340, 0x380.
- Supports direct memory access channels 1 and 3.
- Support of interrupts 3-7, 10-12, 14, 15.
- Availability of a pass-through connector type PC104 + to ensure the convenience of stacks assembly not associated with the elements of the board;
- Ability to create alternative FPGA firmware with support for the changed board functionality. The FPGA firmware can be changed via a dedicated I/O port.

-Possibility of the module to use the following OS:

- Linux 2.6
- QNX6
- FreeDOS
- Windows XP

An example of working with a module without using a library of functions can be found in the file examples/aic324_init.c at FTP server.
Comparative characteristics of the module parameters of different manufacturers in PC/104 form-factor (see ANNEX C).

### 1.2.4 connection of the peripherals

**Table 1: Switching**

| Name on PCB | Function | # of Contacts |
|---|---|---|
| XS1 (PC104) | Connection of PC104 expansion module via ISA bus | 104 |
| XS2 (PC104+) | Pass-through connector; installed for PC104+ system assembly convenience. Not connected to the circuitry of the module. | 120 |
| XP12 (Digital IN/OUT) | 30x digital I/O lines | 34 |
| XP9 (Analog IN/OUT) | 32 analog input lines, 4 analog output lines, 4 digital input lines, 3 digital output lines | 50 |
| XP13 | Interrupt and DMA channel number setting | 30 |
| XP10 | Configuring of ADC input channels types and base address | 10 |
| XP15 | Setting the discrete inputs/outputs group pull-up | 3 |
| XP1 - XP8 | Connection of current measurement resistors to differential ADC channels | 4 |

**Table 2: Light indication**

| Name on PCB | Function | Color |
|---|---|---|
| VD1 (LED1) | User LED | Yellow |

### 1.2.5 Delivery checklist

The delivery checklist includes:

Analog I/O module AIC324;
Antistatic packaging (plastic bag) – 1;
Consumer packaging (cardboard box) – 1.

**Note –** If any of the provided components are missing or have external mechanical damages, please contact the authorized distributor by whom the module was purchased.
Keep the antistatic packaging and consumer packaging of the module in its original form before the end of the warranty period of operation.

# 1.3 Connectors and Ports

## 1.3.1 Analog Connector

**Table 3: XP9 Analog Connector Pinout**

| | | | |
|---|---|---|---|
| AGND | 1 | 2 | AGND |
| Vin0 / 0+ | 3 | 4 | Vin16 / 0- |
| Vin1 / 1+ | 5 | 6 | Vin17 / 1- |
| Vin2 / 2+ | 7 | 8 | Vin18 / 2- |
| Vin3 / 3+ | 9 | 10 | Vin19 / 3- |
| Vin4 / 4+ | 11 | 12 | Vin20 / 4- |
| Vin5 / 5+ | 13 | 14 | Vin21 / 5- |
| Vin6 / 6+ | 15 | 16 | Vin22 / 6- |
| Vin7 / 7+ | 17 | 18 | Vin23 / 7- |
| Vin8 / 8+ | 19 | 20 | Vin24 / 8- |
| Vin9 / 9+ | 21 | 22 | Vin25 / 9- |
| Vin10 / 10+ | 23 | 24 | Vin26 / 10- |
| Vin11 / 11+ | 25 | 26 | Vin27 / 11- |
| Vin12 / 12+ | 27 | 28 | Vin28 / 12- |
| Vin13 / 13+ | 29 | 30 | Vin29 / 13- |
| Vin14 / 14+ | 31 | 32 | Vin30 / 14- |
| Vin15 / 15+ | 33 | 34 | Vin31 / 15- |
| Vout DAC3 | 35 | 36 | Vout DAC2 |
| Vout DAC1 | 37 | 38 | Vout DAC0 |
| Vref out | 39 | 40 | AGND |
| A/D Convertion | 41 | 42 | Ctr2 out/ Dout 2 |
| Dout 1 | 43 | 44 | Ctr0 out/ Dout 0 |
| Extclk/Din 3 | 45 | 46 | ExtGate / Din 2 |
| Gate 0/ Din 1 | 47 | 48 | Clk0 / Din0 |
| +5V | 49 | 50 | DGND |

**Table 4: Designation of the main functional outputs of the XP9 analog connector**

| Name | Function |
|---|---|
| Vin 0/0+ ~ Vin 15/15+ | Analog inputs: 0-15 single-wire inputs/0-15 positive diff. |
| Vin 16/0- ~ Vin 31/15- | Analog inputs: 16-31 single-wire inputs/0-15 neg. diff. |
| Vref out | Reference +5V output. Do not use as power voltage. |
| Vout DAC 0-3 | Analog outputs |
| A/D Conversion | Pulse to start A/D conversion (output) |
| Dout 2- 0 | Galvanically isolated digital outputs combined with a pulse counter |
| Din 3 – 0 | Galvanically isolated digital inputs combined with a pulse counter or ADC startup |
| ExtClk | External ADC startup |
| ExtGate | Input gate latches Ctr 1&2 of 8254 timers module |
| Gate 0 | Input gate latch Ctr0 of 8254 timers module |
| Clk 0 | External clock input for timer 0 (8254 module) operation |
| +5V | Output of galvanically isolated +5V |
| ADND | Analog ground of galvanically isolated analog path |
| DGND | Discrete ground of galvanically isolated analog path |

### 1.3.2. Digital Connector

**Table 5: Pinout of Digital Connector (XP12)**

| | | | |
|---|---|---|---|
| A7 | 1 | 2 | A6 |
| A5 | 3 | 4 | A4 |
| A3 | 5 | 6 | A2 |
| A1 | 7 | 8 | A0 |
| B7 | 9 | 10 | B6 |
| B5 | 11 | 12 | B4 |
| B3 | 13 | 14 | B2 |
| B1 | 15 | 16 | B0 |
| C7 | 17 | 18 | C6 |
| C5 | 19 | 20 | C4 |
| C3 | 21 | 22 | C2 |
| C1 | 23 | 24 | C0 |
| Latch | 25 | 26 | Ack |
| D0 | 27 | 28 | D1 |
| D2 | 29 | 30 | D3 |
| D4 | 31 | 32 | D5 |
| +5V | 33 | 34 | DGND |

**Table 6: Designation of the main functional outputs of the XP12 digital connector**

| Name | Function |
|---|---|
| A7 – A0 | Digital I/O port A |
| B7 – B0 | Digital I/O port B |
| C7 – C0 | Digital I/O port C |
| D5 – D0 | Digital additional I/O port D |
| Latch | Latch input, active level high (port A, mode 1) |
| Ack | Acknowledgement output, active level high (port A, mode 1) |
| +5V | +5V digital power |
| DGND | Digital ground of PC104 bus |

### 1.3.3 Registers Mapping

| | | |
|---|---|---|
| +0 | W | ADC conversion software start |
| If ADC is not in Busy state (AD_BUSY high), writing any value to the register leads to starting ADC conversion. | | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| +0 | R | Reading of the lower data byte from ADC | | | | | | |
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 |
| AD7 – 0 – ADC data from 7 to 0 bits. | | | | | | | | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| +1 | R | Reading of the higher data byte from ADC | | | | | | |
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | AD15 | AD14 | AD13 | AD12 | AD11 | AD10 | AD9 | AD8 |
| AD15 – 8 - ADC data from 15 to 8 bits.<br>*When using 8-bit module access commands, higher byte should be read first, then lower byte. | | | | | | | | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| +2 | R\W | Lower ADC channel number in scan mode. | | | | | | |
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

| Name | x | x | x | CL4 | CL3 | CL2 | CL1 | CL0 |
|---|---|---|---|---|---|---|---|---|
| Lower ADC channel number in scan mode. Writing to this register leads to setting of the channel at the module. Channel number can be from 0 to 31. | | | | | | | | |

| +3 | R\W | Higher ADC channel number in scan mode. | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | x | x | x | CH4 | CH3 | CH2 | CH1 | CH0 |
| Higher ADC channel number in scan mode. Channel number can be from 0 to 31. | | | | | | | | |

| +4 | W | ADC control | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | FIFOEN | ADINTE | SCANEN | x | x | x | x | FIFORST |
| SCANEN (bit 5) – Enable ADC channels scan mode.<br>ADINTE (bit 6) – Enable interrupt from ADC.<br>FIFOEN (bit 7) – Enable FIFO mode when using ADC. If interrupt is enabled, it will occur when TF flag is set to 1. If this mode is disabled and interrupt from ADC is enabled, it will occur each time on ADC conversion.<br>Bit FIFORST – Reset FIFO pointers. | | | | | | | | |

| +4 | R | ADC status | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | FIFOEN | WAIT | STS | 0 | EF | TF | FF | OVR |
| EF, TF, FF, OVF – ADC FIFO status bits: Empty FIFO, FIFO threshold reached, FIFO overflow.<br>STS (bit 5) – ADC status: if = 1 the conversion in process or channels scan mode in process.<br>WAIT (bit 6) = 0 – ADC conversion enabled; = 1 – conversion start is not allowed, the time is needed for setting a signal when a channel is changed, gain or range is switched. The waiting time is about 10 μs. | | | | | | | | |

| +5 | R | DAC status | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DACBUSY |
| DACBUSY bit indicates that data is being transferred to DAC. At this moment writing to the registers 5 and 6 is disabled. | | | | | | | | |

| +5 | W | DAC control | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | WGSTRT | WGPS | WGRST | WGINC | DASIM | DAGEN | DACH1 | DACH0 |
| Bits DACH1-0 set current DAC channel in operation (0 to 3).<br>Bit DAGEN – if = 1, write the set data in FIFO along with the channel number.<br>Bit DASIM – if = 0, when writing Register 5, the data is transferred to DAC and set at DAC output; if = 1, write to buffer occurs without output to DAC.<br>Bit WGINC – Write the data and increment the address counter in buffer. Manual mode.<br>Bit WGRST – Reset the generator buffer address.<br>Bit WGPS – Pause the generator. During pause, bit WGRST can be used to reset the generator.<br>Bit WGSTRT – Generator start in any mode. | | | | | | | | |

| +6 | R | Update DAC data for all 4 channels |
|---|---|---|
| Update DAC data for all 4 channels. | | |

| +6 | W | Write 8 lower DAC bits | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | DAC7 | DAC6 | DAC5 | DAC4 | DAC3 | DAC2 | DAC1 | DAC0 |
| 8 lower DAC bits | | | | | | | | |

| +7 | W | Write 8 higher DAC bits | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | DAC15 | DAC14 | DAC13 | DAC12 | DAC11 | DAC10 | DAC9 | DAC8 |
| 8 higher DAC bits.<br>*Write leads to different results depending on the control bits status.<br>If DASIM = 1, write occurs to memory cell with the DAC channel number, data output to DAC is not done.<br>If DASIM = 0, current written value is additionally sent to DAC.<br>If bit DAGEN = 1, the data are written to FIFO. This write to FIFO operation has priority over DASIM bit. | | | | | | | | |

| +8 | R | Current page and power control | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | 0 | PWREN | 0 | 0 | 0 | P2 | P1 | P0 |
| Bits P2-0 set page for the mode of extended access to the ports of the module. The page consists of 4 registers and is mapped to 12-15 registers of the main IO area.<br>Bit PWREN = 1 – Power is supplied to analog part of the module (default value). | | | | | | | | |

| +8 | W | Setting current page, power and module reset control | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | 0 | PWREN | INTRST | RESETD | RESETA | P2 | P1 | P0 |
| Bits P2-0 set page for the mode of extended access to the ports of the module. The page consists of 4 registers and is mapped to 12-15 registers of the main IO area.<br>Bit RESETA – Reset of DAC, FIFO, DIO and all internal registers. 8254 timer(s) is not reset.<br>Bit RESETD – The same reset as RESETA, but DAC is not affected.<br>Bit INTRST – Interrupts reset.<br>Bit PWREN = 1– Power is supplied to analog part of the module (default value). | | | | | | | | |

| +9 | R | Read galvanically isolated digital inputs | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | 0 | 0 | Debounce | DINTE | DIN3 | DIN2 | DIN1 | DIN0 |
| Bits DIN3-0 – Read digital inputs at analog connector.<br>Bit DINTE – Enable interrupt from digital IO.<br>Bit Debounce – Enable software debounce at Din[3] input. In case of bad signal, leads to possibility of the interrupt setting jitter of 6.4 µs max. | | | | | | | | |

| +9 | W | Isolated digital outputs control | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | x | x | Debounce | DINTE | LED | DOUT2 | DOUT1 | DOUT0 |
| Bits DOUT2-0 – Control of digital outputs at analog connector.<br>Bit LED = 1, – Switch on the VD1 onboard LED.<br>Bit DINTE – Enable interrupt from digital IO.<br>Bit Debounce – Enable software debounce at Din[3] input. In case of bad signal, leads to possibility of the interrupt setting jitter of 6.4 µs max. | | | | | | | | |

| +10 | R\W | Timer 8254: clock and signal source control | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | TINTE | GT12EN | SRC0 | GT0EN | OUT0EN | OUT2EN | FREQ0 | FREQ12 |
| Bit FREQ12 = 1, – Counter 1 input is supplied with 200 kHz signal from the internal generator; if = 0 – 20 MHz is supplied from the same source.<br>Bit FREQ0 = 1, – Counter 0 input is supplied with 20 kHz signal from the internal generator; if = 0 – 20 MHz is supplied from the same source.<br>Bit OUT2EN = 1, – Counter 2 output is routed to OUT2\DOUT2 output, cont. 42 of XP9 conn.<br>Bit OUT0EN = 1, – Counter 0 output is routed to OUT0\DOUT0 output, cont. 44 of XP9 conn.<br>Bit GT0EN =1, – Gate0\DIN1 (cont. 47 of XP9) connected to timer 0. Active level is high. Pull-up to power 10 kOhm.<br>Bit SRC0 = 1, – Timer 0 receives clock freq. from FREQ0. = 0 – Clock input of the timer is connected to pin CLK0\DIN0 (cont. 48 of XP9). Active edge is negative. Pull-up to power 10 kOhm.<br>Bit GT12EN =1 and if ExtGate\DIN2 (cont. 46 of XP9) = 0, then ADC conversion is started. ADC conversion is not started, if this pin = 1. If it was 0 at start and then set to 1, conversion pause is set until it is 1. Pull-up to power 10 kOhm.<br>Bit TINTE – Enable interrupt from 8254 timer. | | | | | | | | |

| +11 | R\W | Interrupt flags read and reset | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | x | x | x | x | x | ADINT | TINT | DINT |
| Bit DINT = 1, interrupt received from discrete IO.<br>Bit TINT = 1, interrupt received from 8254 timer.<br>Bit ADINT = 1, interrupt received from ADC.<br>Writing 1 in the correspondent bit resets the flag. To reset all flags, write 0xFF. | | | | | | | | |

### 1.3.4 Page 0 – 8254 Timer

| +12 | R\W | Read/write counter 0 data |
|---|---|---|
| +13 | R\W | Read/write counter 1 data |
| +14 | R\W | Read/write counter 2 data |
| +15 | R\W | 8254 counter control port |

Operation modes and registers fully comply with 8254 timer counter. For details, see standard description, for example at: http://www.digchip.com/datasheets/parts/datasheet/227/8254.php

### 1.3.5 Page 1 – Input / Output port 8255

| | | |
|---|---|---|
| +12 | R\W | Port A read/write |
| +13 | R\W | Port B read/write |
| +14 | R\W | Port C read/write |
| +15 | R\W | Control port read/write |

Operating modes and registers fully comply with the Intel 8255 microchip. For details, see the standard description, e.g.: http://en.wikipedia.org/wiki/Intel_8255

**ATTENTION!** All the ports support the 0 port. The 1 mode is supported only by A port, external synchronization outputs during operation in the 1 mode are routed to separate outputs of digital connector and not to the C port as described in the configuration of the 8255 chip.

**ATTENTION!** Additional digital port D has the direction of data transfer related to the port C 8255. i.e. Outputs D3 – D0 have the similar direction with the lower part of the port C (C3 –C0), outputs D5 – D4 have the similar direction with the upper part of the port C (C7 –C4).

### 1.3.6 Page 2 – ADC control

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| +12 | W | The least significant byte of the infill ratio for FIFO | | | | | | |
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | FT8 | FT7 | FT6 | FT5 | FT4 | FT3 | FT2 | FT1 |
| Bits FT8-1 FIFO threshold during which interrupt is generated for ADC data acquisition from FIFO. | | | | | | | | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| +12 | R | The least significant byte of threshold value for FIFO | | | | | | |
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | FC7 | FC6 | FC5 | FC4 | FC3 | FC2 | FC1 | FC0 |
| Bits FC7-0 the least significant byte of the word, specifying the current amount of data in FIFO. | | | | | | | | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| +13 | R\W | The most significant address of threshold value for FIFO | | | | | | |
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | x | x | x | x | x | x | FT10 | FT9 |
| Bits FT10 – 9 FIFO threshold at which generation of interrupt for ADC data acquisition from FIFO is carried out. FIFO size amounts to 2048 words. | | | | | | | | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| +13 | R | The most significant byte of FIFO infill ratio | | | | | | |
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | 0 | 0 | 0 | 0 | FC11 | FC10 | FC9 | FC8 |
| Bits FC11 – 8 the most significant byte of the word, specifying the current amount of data in FIFO. FIFO amounts to 2048 words. | | | | | | | | |

| +14 | R\W | Control of ADC clocking | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | x | x | x | x | x | CLKSEL | CLKEN | DMAEN |
| Bit DMAEN resolution for DMA channel operation at ADC data acquisition with the use of FIFO.<br>Bit CLKEN pclocking resolution of ADC conversion start. If bit = 0, then ADC start is possible only by writing to the relevant bit of the board register.<br>Bit CLKSEL = 0, ADC start over the negative edge from the DIN3\EXTCLK output. =1, start over the negative edge from the output of timer/counter 2 8254. The counter 2 functions together with the counter 1 8254. | | | | | | | | |

| +15 | R\W | Configuration of ADC conversion parameters | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | RANGE | ADBU | G1 | G0 | SCINT1 | SCINT0 | S\D1 | S\D0 |
| Bits S\D1-0 define operation mode of ADC ingress switches. 0 – differential inputs, 1 – standard inputs. Bit 0 sets the configurations for 0-7 and 16-23 channels, bit 1 – 8-15 and 24-31. Bit 0 – is controlled by jumper J21, bit 1 – J22. Jumper's position "open" corresponds to the logical unit.<br>Bits SCINT1-0 set the interval of channel switching in scanning mode.00 – 20 μs, 01 – 15 μs, 10 – 10 μs, 11 – 4 μs.<br>Bits G1-G0 set the gain ratio of ADC path from 1 to 8.<br>Bits RANGE and ADBU set the ADC operation mode.<br>RANGE = 1 range of ADC conversion 10V, =0 range of ADC conversion to 5V.<br>ADBU = 0 bipolar conversion mode, = 1 unipolar conversion mode. | | | | | | | | |

### 1.3.7 Page 4 – additional digital port

| +12 | R | Reading the FPGA outputs from the additional D port | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | 0 | 0 | D5 | D4 | D3 | D2 | D1 | D0 |
| Bits D5-0 reading the state of the FPGA outputs of the additional D port. Direction of I/O of the D port is defined by the direction of output of the most significant and the least significant registers of the C 8255 port. Direction of the C port of the lower part determines the direction of operation for the D3..0 registers. The direction of the C port of the upper part determines direction of the operation for registers D5..4.  | | | | | | | | |

| +12 | W | Writing data to additional port D | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | x | x | D5 | D4 | D3 | D2 | D1 | D0 |
| Bits D5-0 writing to the additional port D. The direction of input/output of port D output is determined by the direction of output of the upper and lower registers of port C 8255. The direction of the C port of the lower part determines the direction of work for registers D3..0. The direction of C port of the upper part determines the direction of work for registers D5..4. | | | | | | | | |

### 1.3.8 Page 5 – DAC control

| +12 | R\W | Lower address of the DAC buffer | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit# | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | DACA7 | DACA6 | DACA5 | DACA4 | DACA3 | DACA2 | DACA1 | DACA0 |
| Bits DACA7-0 Address for writing the DAC data to the circular signal generation buffer with the use of DAC. Buffer length is 1024 DAC readouts. Code and number of DAC channel are written. | | | | | | | | |

| +13 | R\W | Upper address of DAC buffer | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | x | x | x | x | x | x | DACA9 | DACA8 |
| Bits DACA9-8 Address for writing the DAC data to the circular buffer of signal generator with the use of the DAC. Buffer length amounts to 1024 DAC readouts. Code and number of DAC channel are written. | | | | | | | | |

| +14 | R\W | Configuration of the operation mode of signal generator (DAG) | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | WGSRC 1 | WGSRC 0 | WGCH1 | WGCH0 | DEPTH3 | DEPTH2 | DEPTH1 | DEPTH0 |
| Bits DEPTH 3-0 Define the buffer size used. Depth = [DEPTH(3-0)+1]*64.<br>Bits WGCH1-0 Define the number of words to be transferred at a single session to DAC. 00 – 1 word, 01 – 2 words, 1x – 4 words.<br>Bits WGSRC 1-0 Define DAC clocking source. 00 – manual, using the WGINC register, 01 – output of counter 0 8254, 10 – output of counter 12 8254, 11 – external, foot 45. | | | | | | | | |

| +15 | R\W | Установка конфигурации ЦАП | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | | DAC_off | DAG1_1 | DAG1_0 | DAG0_1 | DAG0_0 | DAPOL1 | DAPOL0 |
| Bits DAPOL1-0 = 1, bipolar output DAC 2-3 and 0-1, respectively.<br>Bit DAG1_1-0 (DAG0_1-0) – selection of the DAC conversion range 2-3 (0-1). 00 – 5V, 01 – 10V, 10 – 20V, 11 – DAC is enabled. * also see the rules for range switching.<br>Bit DAC_OFF – setting the bit to one leads to the disabling outputs from DAC and their PE via 10 kOhm. | | | | | | | | |

* Rules for switching the DAC ranges

| DAC output voltage, V | Conversion range, V | DAG [1:0] | DAPOL |
|---|---|---|---|
| 0..5 V | 5 | [00] | 0 |
| 0..10 V | 10 | [01] | 0 |
| ±2,5 V | 5 | [00] | 1 |
| ±5 V | 10 | [01] | 1 |
| ±10 V | 20 | [10] | 1 |

### 1.3.9 Summary table of registers

| Base + | Read | Write |
|---|---|---|
| +0 | Reading ADC data, the least significant byte | Software-based start of ADC conversion. |
| +1 | Reading ADC data, the most significant byte | |
| +2 | Minor number of ADC channel in the scanning mode | Minor number of ADC channel in the scanning mode |
| +3 | Major number of ADC channel in the scanning mode | Major number of ADC channel in the scanning mode |
| +4 | FIFO flags + ADC state | ADC control |
| +5 | DAC state | DAC control |
| +6 | Data update in all the 4 DAC channels. | The least significant byte of DAC |
| +7 | The most significant DAC byte | |
| +8 | Current page | Board control system |
| +9 | Digital port reading | Control of interrupts and digital port |
| +10 | State of the 8254 timer | Control of inputs/outputs of 8254 |

| | | |
|---|---|---|
| | | timer |
| +11 | Interrupt flags | Reset of interrupt flags |
| ***Page 0 8254 timer*** | | |
| +12 | Counter 0 data reading | Counter 0 Data writing |
| +13 | Counter 1 data reading | Counter 1 data writing |
| +14 | Counter 2 data reading | Counter 2 data writing |
| +15 | Control port reading | Control port writing |
| ***Page 1 8255 I/O port*** | | |
| +12 | Port A reading | Port A writing |
| +13 | Port B reading | Port B writing |

| | | |
|---|---|---|
| Base + Reading Writing +14 | Port C reading | Port C writing |
| +15 | Control port reading | Control port writing |
| ***Page 2 ADC control*** | | |
| +12 | Minor FIFO address | Minor FIFO address |
| +13 | Major FIFO address | Major FIFO address |
| +14 | ADC clocking control | ADC clocking control |
| +15 | Configuration of ADC parameters | Configuration of ADC parameters |
| ***Page 3 Access to calibration parameters*** | | |
| ***Page 4 Additional digital port*** | | |
| +12 | Reading additional digital port | Writing additional digital port |
| ***Page 5 DAC control*** | | |
| +12 | Minor address of DAC buffer | Minor address of DAC buffer |
| +13 | Major address of DAC buffer | Major address of DAC buffer |
| +14 | DAC operation modes | DAC operation modes |
| +15 | Configuration of DAC outputs | Configuration of DAC outputs |
| ***Page 6 Programming FPGA boot loader*** | | |

## 1.4 LABELING

In accordance with the requirements of the design documentation, the module's labeling is applied to the printed circuit board and contains the following symbols:

- Conventional name (code) of the module;
- Name of the manufacturer;
- Serial number of the card;
- Year of commencement of serial production;
- Decimal number of the printed circuit board;
- Positional designations of elements.

The labeling of the consumer packaging is performed by sticking the individual identifier (sticker) of the module implementation version.

The box sticker contains the following symbols:

- Name of the module's version;
- Designation of the module's version in the Fastwel® product catalog.

## 1.5 PACKAGING

In accordance with the requirements of the manufacturing specifications, the module is packed in an individual anti-static package (package) and placed in a separate consumer container (cardboard box).

The inner cardboard insert inside the consumer packaging provides additional strength, prevents deformation and displacement of the module during transportation.

# 2 INTENDED USE

## 2.1 PREPARATION FOR USE

### 2.1.1 Information on the types of hazardous exposures

Module's design makes it safe for human life and health when used under specified operating conditions. The module contains no sources of hazardous exposures.

### 2.1.2 General requirements

All installation and preparation works with the module and the devices connected to it should be carried out only when the power supply of the devices is switched off and there are no voltages on the module connectors.

**ATTENTION: THE GENERAL REQUIREMENTS FOR THE PREPARATION OF THE MODULE'S USE SHOULD BE STRICTLY FOLLOWED TO AVOID BREAKDOWN OF THE MODULE'S OUTLET!**

### 2.1.3 ESD requirement

In accordance with GOST R IEC 60950-2002 (for equipment connected to the mains with a voltage up to 600 V). All assembly and preparation works, replacement of the components and module maintenance should be performed only with the use of special tools and hardware (for example, ESD straps etc.), free of the electrostatic discharge of and magnetization properties.

**ATTENTION: THE MODULE CONTAINS ESD COMPONENTS!**

### 2.1.4 Module installation

Prior to start working with the module, you should:

- inspect module's structure and carefully read this user manual;
- set the jumpers in accordance with the required values (see the Annex B2)
- connect XS1 of the module with the CPU module's connector;
- connect mating parts to XP9 and XP12 connectors, if necessary

**Note –** Location of the main components and connectors of the module is given in p.1.2.1.

### 2.1.5 Module's firmware update

To update the module's firmware you could use the "aicfw" utility, which is a freeware and can be found in manufacturer's networks resources and is designed for the following operating systems: DOS, Linux, Windows, QNX6.

Windows-version of this utility program requires installation of a system driver, which can be found in archives together with the utility program. The driver is installed in the usual manner, using the installation wizard.

After installing the system driver, you need to set the module resources (base address and interrupt number) in accordance with the jumper configuration using the standard Device Manager program.

After unpacking the archive, copy to the target system the executable file "aicfw" and the "xsvf" - file for updating the firmware of the module corresponding to the operating system, run the system command interpreter, change the current directory to the directory with the executable file, then execute the command with the admin account rights:

./aicfw -p 0x <module base address> <path to the xsvf-file of the firmware>, or

aicfw.exe -p 0x <base address of the module> <path to the xsvf-file of the firmware>

After the upgrade process is completed, you must restart the module by removing the power supply.

## 2.2 USE OF THE MODULE

During operation, the module is automatically configured and does not require any adjustments and software settings.

# 3 MAINTENANCE

The module does not require maintenance for the entire service life.

# 4 REPAIRS

The module should be repaired only in the Service Centers of the manufacturer or in the authorized Service Centers of FASTWEL®.

The main provisions and the grounds for carrying out repairs are set out in Section 8 of the User Manual.

**ATTENTION: ANY INDEPENDENT REPAIRS ON THE MODULE BY USERS IS PROHIBITED!**

# 5 STORAGE

## 5.1 STORAGE CONDITIONS

Module’s storage conditions 1 is in accordance with the GOST 15150-69.

# 6 TRANSPORTATION

## 6.1 GENERAL REQUIREMENTS AND CONDITIONS

### 6.1.1 Transport packaging

The module should be transported in a separate packaging box (transport packaging) of the manufacturing facility, which consists of an individual antistatic bag and a cardboard box.
It is possible to transport the modules, packaged in individual antistatic packages, in multiple packaging (transport packaging) of the manufacturing facility.
The packaged modules should be transported in accordance with the shipping rules, operating with this particular type of transport.
During handling and transportation operations, the packaged modules should not undergo sharp pounding, falls, shocks and exposure to atmospheric precipitation. The packaged modules should be stored in a carrier vehicle in such a manner which will prevent their moving.

**ATTENTION: PROTECTION OF MODULE'S TRANSPORT PACKAGING AGAINST DIRECT EXPOSURE OF ATMOSPHERIC PRECIPITATIONS SHOULD BE ENSURED!**

### 6.1.2 Transportation means

The modules can be transported by automobiles and by railway, without any speed limitations and over all distances.

Transportation by air is allowed in heated and pressurized compartments over all distances.

### 6.1.3 Climatic conditions

The modules can be transported by the above transport types under the following climatic conditions:

Ambient air temperature from -50 to +60 °C;
Relative humidity is no more than 95 % at the temperature up to +30 °C;
Atmospheric pressure is from 84 to 107 kPa (from 630 to 800 mm Hg.).

## 6.2 TRANSPORTATION CHARASTERISTICS

**Dimensions:**

Overall dimensions of the shipping container, no more than: 155x140x45 mm.

Weight**:** no more than 0.12 kg.

Weight of the shipping container, no more than: 0.1 kg.

## 6.3 PLACEMENT AND FIXING THE SHIPPING CONTAINER

Placement and fixing of the shipping container should ensure stability of its position, excluding displacements and impacts during transportation.

**ATTENTION: DURING TRANSPORTATION, ANY JOLTS, DROPS OR IMPACTS SHOULD BE AVOIDED, SINCE THEY COULD HAVE AN EFFECT ON THE SAFETY AND WORKING EFFICIENCY OF THE MODULE!**

# 7 UNPACKING

## 7.1 GENERAL REQUIREMENTS AND CONDITIONS

### 7.1.1 Climatic requirements

The module should be unpacked only in the area at the ambient temperature of no less than +15° C and a relative humidity of no more than 70 %.

### 7.1.2 Additional requirements

Unpacking the module, which was at an ambient temperature below 0° C, should only be performed in a heated room, after having the module stored under normal conditions for 6 hours.

**ATTENTION: PLACEMENT OF THE PACKAGED MODULES NEAR A HEAT SOURCE IS PROHIBITED!**

### 7.1.3 Safety precautions

When unpacking the module, all precautions necessary to ensure its safety should be observed.

### 7.1.4 Assessment of external view

At the time of unpacking it is required to check the module that it has no external mechanical damages after transportation.

**ATTENTION –** If any of the components of the delivery checklist are missing or have external mechanical damages, contact the authorized distributor by whom the module was purchased.

Please keep the marketable condition of consumer packaging (bag) of the manufacturing company till the end of the warranty period.

# ANNEX A

**(provided for reference)**

## List of the abbreviations and notations used

Module – analog and digital I/O module AIC324;

FASTWEL® –Fastwel® company, official distributor;

UM or Manual – User Manual;

# ANNEX B

## (Mandatory)

## Functions of jumpers of AIC324

| Jumper | Function |
|---|---|
| J1 | DACK3 |
| J2 | DRQ3 |
| J3 | DACK1 |
| J4 | DRQ1 |
| J5 | IRQ7 |
| J6 | IRQ6 |
| J7 | IRQ5 |
| J8 | IRQ4 |
| J9 | Pulling-up interrupts. Is set if the board is the only board on this interrupt. |
| J10 | IRQ3 |
| J11 | IRQ14 |
| J12 | IRQ15 |
| J13 | IRQ12 |
| J14 | IRQ11 |
| J15 | IRQ10 |
| J16 | A0, setting the base address of the board |
| J17 | A1, setting the base address of the board |
| J18 | A2, setting the base address of the board |
| XP15 | Pulling-up digital inputs-outputs, position 1-2 to power supply, position 2-3 to earth. |
| J21 | Bit SD0 register conf. ADC, page 2, register 15 log. “1” if the jumper is not set. |
| J22 | Bit SD1 register conf. ADC, page 2, register 15 log. “1” if the jumper is not set. |

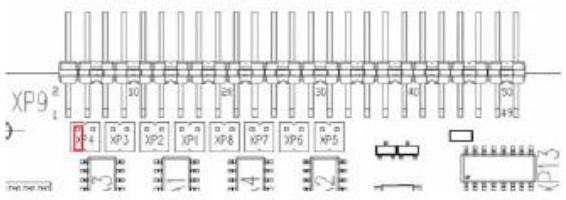
Selection of the board base address

| J16 | J17 | J18 | Base address (hex) |
|---|---|---|---|
| - | + | - | 0x100 |
| - | - | - | 0x140 |
| + | + | - | 0x180 |
| - | - | + | 0x200 |
| + | - | + | 0x280 |
| - | + | + | 0x300 |
| + | - | - | 0x340 |
| + | + | + | 0x380 |

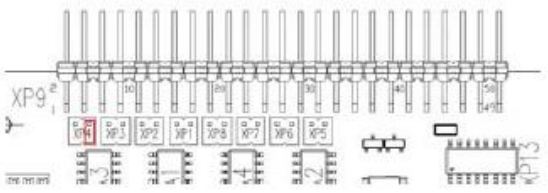
“+” – jumper is set, “-“ – jumper is not set.

Setting the jumpers for enabling the current measurement mode. The current is measured only in the differential mode of the board operation.

Position of 1-2 XP4 jumper



Position of 3-4 XP4 jumper



Positions of jumpers for the current measurement modes.

| Jumper | XP4 | | XP3 | | XP2 | | XP1 | | XP8 | | XP7 | | XP6 | | XP5 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Position | 1-2 | 3-4 | 1-2 | 3-4 | 1-2 | 3-4 | 1-2 | 3-4 | 1-2 | 3-4 | 1-2 | 3-4 | 1-2 | 3-4 | 1-2 | 3-4 |
| ADC channel number | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |

# ANNEX C
**(provided for reference)**

**Comparative characteristics of the parameters of modules by various manufacturers made in PC/104 form-factor**

| | AIC324 (Fastwel | DMM32DX-AT (Diamond) | STX104 (Apex Embedded System) | Model 526 (Sensoray) | DM6430HR-1 (RTD) |
|---|---|---|---|---|---|
| **Bus** | PC104 | PC104 | PC104 | PC104 | PC104 |
| **ADC** | 16 bit | 16 bit | 16 bit | 16 bit | 16 bit |
| **Conversion frequency, kHz** | 250 | 250 | 200 | 40 | 100 |
| **SINAD** | 90 dB | 87 dB | | 95 dB | |
| **Number of channels** | 32/16 | 32/16 | 16/8 | 8 | 16/8 |
| **Differential outputs** | + | + | + | | + |
| **Range of input voltages, V** | ±10…±0.625 +10…+0.625 | ±10…±0.625 +10…+0.625 | ±10…±1,25 | ±10 | ±10…±1,25 |
| **Reception of current signals** | 0..20, 0..10, 0..5 mA | - | - | - | - |
| **DAC** | 16 bit | 16 bit | 16 bit | 16 bit | 16 bit |
| **Inst. time** | 6 µs | 6 µs | | 100 µs | 100 µs |
| **Number of channels** | 4 | 4 | 2 | 4 | 2 |
| **Output voltage** | ±10V…±2.5 V +10V…+5V | ±10V…±2.5V +10V…+5V | ±10V…±5V | ±10V | ±10V |
| **Output current** | 3 mA | 5 mA | | 2 mA | 5 mA |
| **Nonlinearity** | ±1 LSB | ±1 LSB | ±1 LSB | | |
| **Digital I/O** | 30 | 24 | 4 | | 16 |
| **Number of lines in a group** | 4/8 | 4/8 | | | 8 |
| **Counters** | 16 + 32 bit | 16 + 32 bit | 32 | | 16 + 16 bit |
| **Load capacity** | ±50 mA | ±35 mA | ±12 mA | ±20 mA | ±12 mA |
| **Output levels** | 5V CMOS | 5 V | 5 V | | TTL |
| **ESD** | - | - | - | | - |
| **Power supply** | +5 V | +5 V | +5 V | +5 V | +5 V |
| **Consumption** | 600 mA | 410 mA | | 280 mA | 700 mA |
| **Temperature** | -40+85°C | -40+85°C | -40+85°C | 0 .. +70°C | -40+85°C |

# ANNEX D

## DISCLAIMER

This Disclaimer contains special operating conditions of Fastwel in the following areas: intellectual property, warranty policy, conditions of the order and delivery.

### 1 INTELLECTUAL PRORETY

1.1 If any infraction, interference, improper use, illegitimate exploitation and/or violation of the industrial and/or intellectual property rights of any third party and/or property, exploitation during the use of Fastwel Embedded Module will take place – Fastwel does not guarantee to replace the materials, computer programs, procedures or equipment affected by the complaint and under no circumstances doesn't bear responsibility in any form for possible refusal in case of such a replacement.
1.2 Use of the Fastwel products as well as the objects of intellectual property containing in them, in the ways and for the purposes, not provided by the present user manual and datasheet isn't allowed without preliminary written approval of Fastwel.
1.3 Fastwel is not responsible for possible incidents and losses, related to the operation of end devices, in which the original Fastwel equipment is used.

### 2 WARRANTY POLICY

2.1 When the detected flaws in an element can be corrected without decreasing the foreseen technical features and functionality for it, User may demand Fastwel the urgent correction of the failures in additionally agreed period and an increasing of the period of the guarantee of the element equal as the time elapsed from the formal request to repair the failures, until the receipt of the repaired element. All costs associated to the correction of failures, included those of assembly, dismantle, transport, tests, etc, if they exist, shall be prosecuted according the Warranty Policy of Fastwel.

### 3 ORDER AND DELIVERY CONDITIONS

3.1 The general rule is that all Fastwel equipment prices are determined with due consideration of delivery under the EXW terms and conditions (Incoterms 2010). Delivery of the products under other terms and conditions should be preliminary agreed and stated in writing between the parties.
3.2 Unless otherwise expressly agreed with Fastwel, all the deliveries of Fastwel equipment will be carried out only after the official purchase order is obtained and provided that the ordered products have been prepaid in full. Other terms and conditions of cooperation should be made in writing.
3.3 Any delivery of Fastwel electronics is submitted with the right package in accordance with the current rules and standards in the Member States of the European Economic Area. The purchaser independently bears all risks regarding the compliance of package and marking of Fastwel products with legislation requirements being in effect at the place of purchased products destination (in the buyer's country). The specified condition excludes unequivocally any liability of Fastwel for possible non-compliance of package and marking of products with the requirements of legislation of the country of products destination.
3.4 In general, all components of the supply are properly protected with respect to freight, in order to avoid any damage to the supply, third parties, environmental damages or unrelated goods, as consequence of wrong packaging.
3.5 Each package unit is labeled on the exterior area with the indications of product's Part Number and Serial Number.
3.6 The support documents for the order should be made either in English or in Russian unless otherwise agreed between parties in writing.
3.7 Fastwel does not pay penalties and does not cover costs associated with delay in the delivery of the products caused by actions of the third parties, force-majeure etc. - Fastwel doesn't bear any responsibility for non-execution or inadequate execution of the obligations in a case when it is caused by actions of the third parties (for example producers or suppliers of accessories), force majeure etc.
3.8 Fastwel declares that independently and at any time without damage, it has an exclusive right to define and change functionality architecture, bill of materials of its products without any preliminary coordination and approvals of the third parties.

### 4 OTHER CONDITIONS

4.1 Fastwel has the obligation to respect the current Russian legislation (including, but not limited to environmental, labor, social laws) in each moment and to apply it to its embedded electronics considering all and each execution phase, that is to say, from the design until the commissioning and subsequent maintenance. In this regard Fastwel is not liable to the user or other persons in connection with possible changes of the company's rules (including, but not limited to warranty, ordering policy) caused by changes of the Russian legislation.
4.2 Unless otherwise expressly agreed in writing, Fastwel provides no training for assembly\installation\adjustment\operation of its equipment.